KEKB Control System

for KEKB Accelerator Review Committee

February 24, 2001 by Tadahiko Katoh

1. Work done since last Accelerator Review Committee

A. Application programs written for KEKB commissioning and operation.

	Present	Last Year	
medm files	88*	74	* more than this number.
sad files	231	141	
tcl/tk files	2	2	
python files	47	42	
Others	4	4	Java, C/C++, UNIX Commands

B. Configuration change of acsad server workstations.

New Compaq server workstation was introduced as acsad3 due to the new rental contract of the central computer system of KEK.

Name	OS	Specfp95	SpecInt95	# of CPUs	
acsad2	V5.1	20.8	18.4	4	
~~acsad3~~	~~V4.0~~	~~12 *~~	~~9 *~~	~~6~~	(*very rough estimate)
acsad3	**V5.1**	**77.0**	**36.4**	**4**	
acsad4	V5.1	57.7	27.3	3	

The total computing capabilities becomes, 564.3 Specfp95 and 301.1 SpecInt95 instead of 328.3 and 209.5 respectively.

C. Survey of hardware errors occurred in the BPM IOCs.

There still exist problems in the BPM IOCs that force us to reset and reboot an IOCs frequently. The statistics of the number of re-boots is shown in Fig. 1. These data are taken by KEKB Beam Monitor Group. We have tried to solve the problem and to get more stable operation of the system. Recently we found that the abnormal VME bus cycle occurs with certain combination of the VME modules. It happens once in several hours at the test bench that consists of a Schroff VME subrack, a Mitsubishi system monitor module, a National Instruments VME-MXI bus driver module, and a Schroff power supply module. Several types of the CPU modules have been tested and it was found that the VME-MXI bus driver module generates an abnormal

DTACK* signal during the bus handshake sequences. The responses of the CPU modules are different due to the CPU architecture and PCI-VME bus-bridge LSI versions. We tested CPU modules listed below. The normal and abnormal bus signals are shown in Fig. 2. Examples of the FORCE CPU64 and PowerCore 6750 cases are shown in Figs. 3 and 4. We expect this problem will be fixed in the near future.

CPU Modules tested

FORCE CPU40: MC68040, 33 MHz
FORCE CPU64: MC68060, 66 MHz
FORCE PowerCore 6603: PPC 603, Universe Chip
FORCE PowerCore 6750: PPC 750, 266 MHz, with Universe II Chip
FORCE PowerCore 6750: PPC 750, 400 MHz, Universe IIB Chip

2. Work planned in the next one year.

A. PF-AR Accelerator Control System

PF-AR(Photon Factory Advanced Ring) is scheduled to be shut down next week and large modification will be done by the end of this year. The ring is currently operated by a control computer system of 20 years old. The system was a part of TRISTAN control computer system. Some accelerator components will be replaced with new ones and the control computer system will also be replaced by a new one based on EPICS. We will reuse CAMAC modules and the serial highways again as we did in the case of KEKB. In the new system, a new faster server workstation will be introduced with larger RAID disk drives. The server workstation will be used both for PF-AR and KEKB operations and software development. We will add 8 IOCs for PF-AR as Fig. 5. Principal specifications are listed below.

Name	Processor Chip & Clock Freq.	Memory	Disk	RAID Disk
abco1	PA-RISC 8000, 180 MHz x 4	2 GB	13 GB	20 GB
abco2	PA-RISC 8500, 440 MHz x 2	1 GB	18 GB	200 GB

B. Console Desks in the Central Control Room

When the control system for PF-AR will be replaced, the operators' console will also be replaced by the modern PCs and X-terminals using TFT LCDs (Thin-Film-Transistor Liquid Crystal Display). Then, we will be able to make the Central Control Room so flexible that we can easily modify or arrange consoles for satisfying requirements.

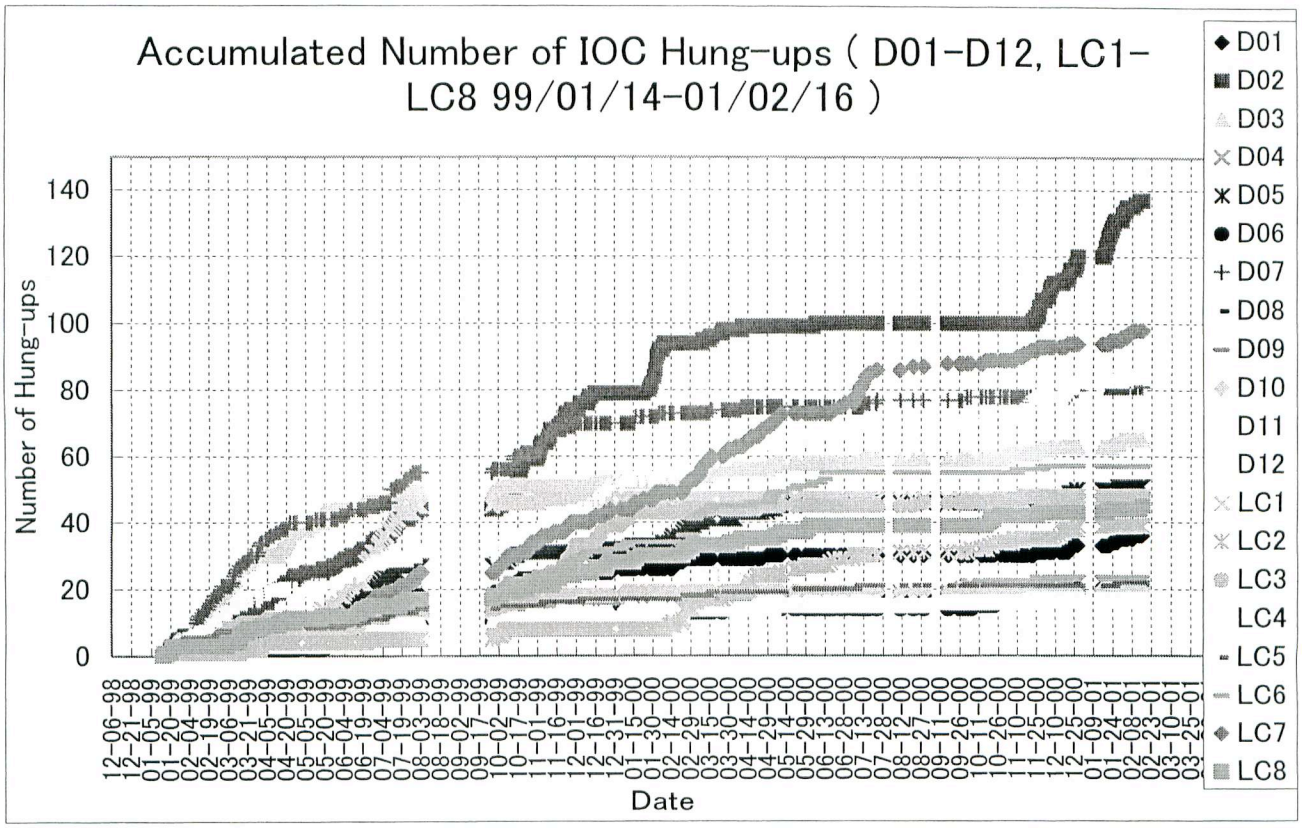


Fig. 1. Accumulated number of Hung-ups of BPM IOCs.

PowerCore 6750, 266 MHz, with Universe Chip

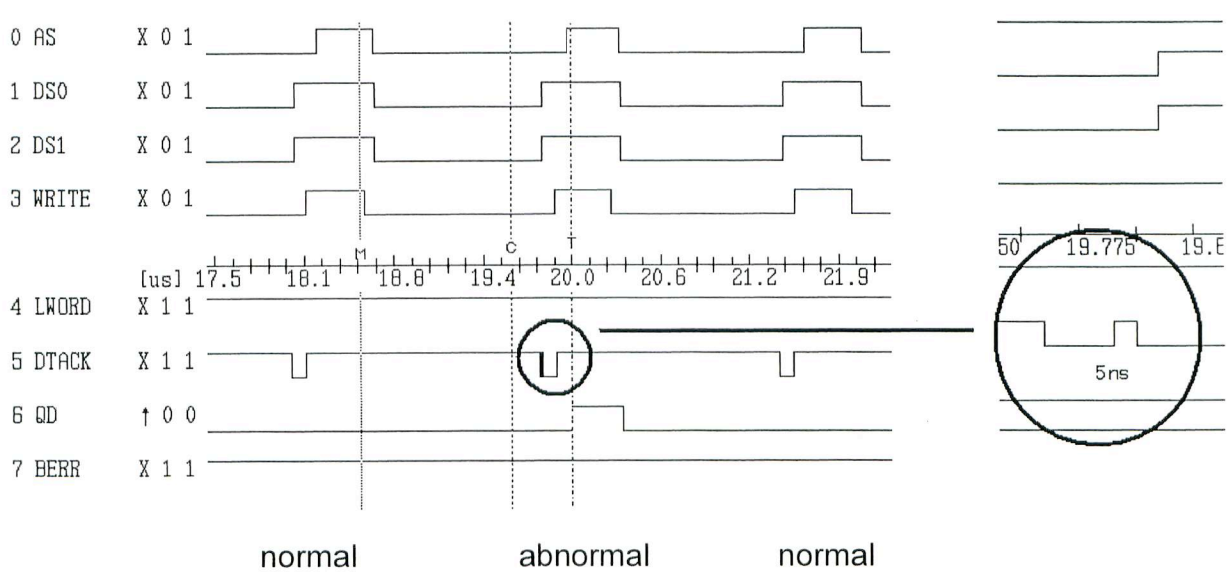


Fig. 2. Normal and abnormal DTACK* bus signals on the VME bus.

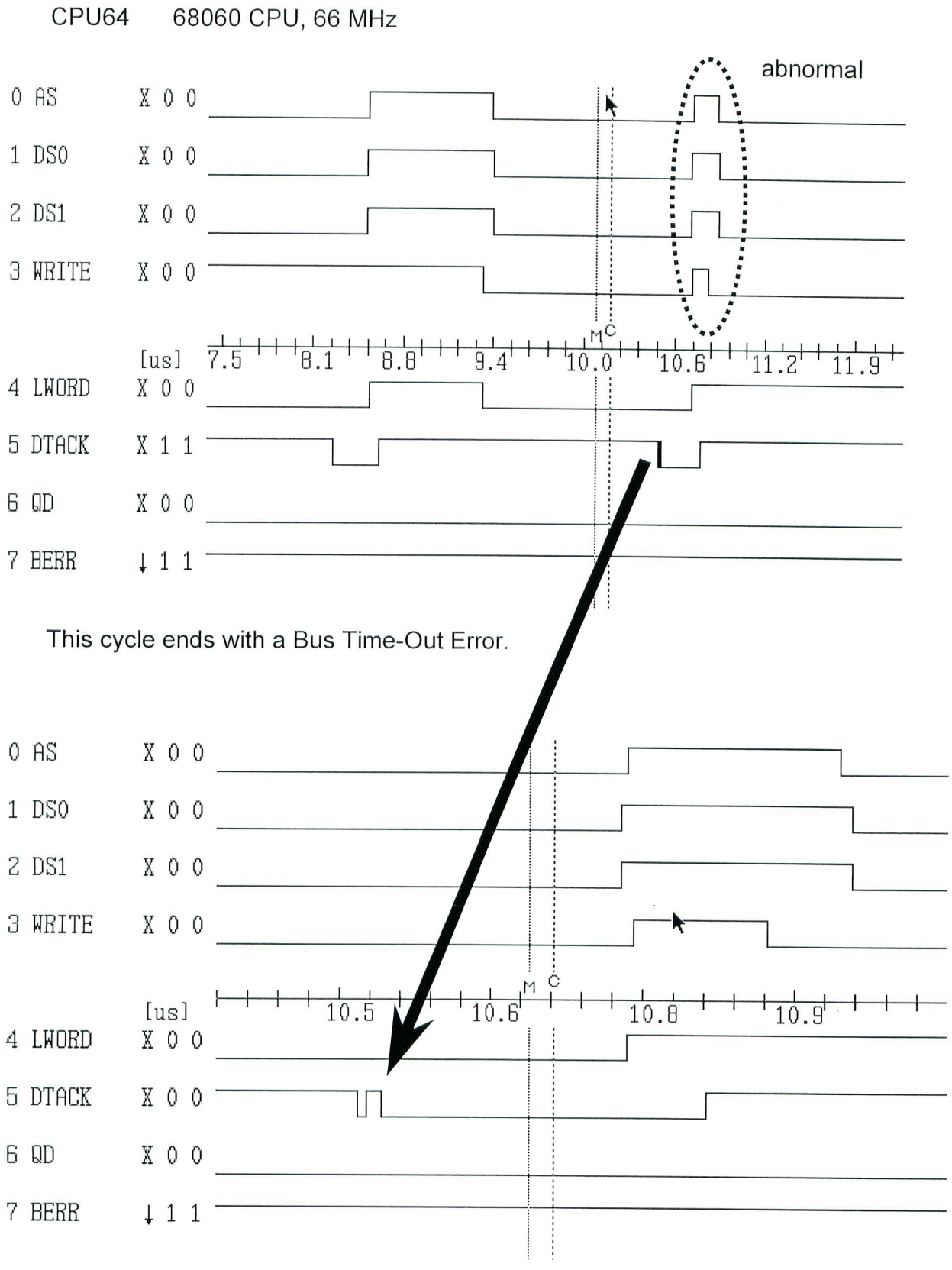
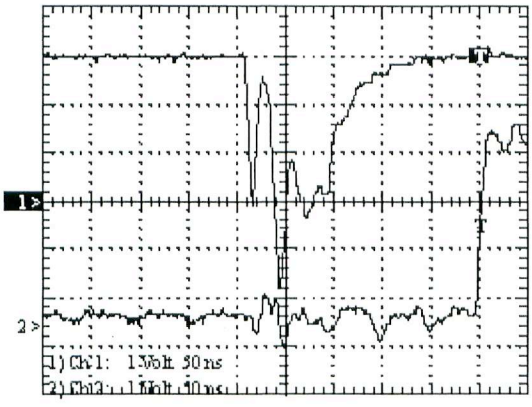


Fig. 3. Abnormal VME bus cycle with a CPU64 and a VME-MXI driver.

PowerCore 6750, 400 MHz, with Universe IIB in FORCE subrack



DTACK* Wave Form with the trigger signal QD. QD is generated by a re-triggerable Flip-Flop triggered by AS*. It indicates that AS* did not return to high state.

Fig. 4a. Abnormal wave form of the DTACK* signal on the VME bus

PowerCore 6750, 400 MHz, Universe IIB

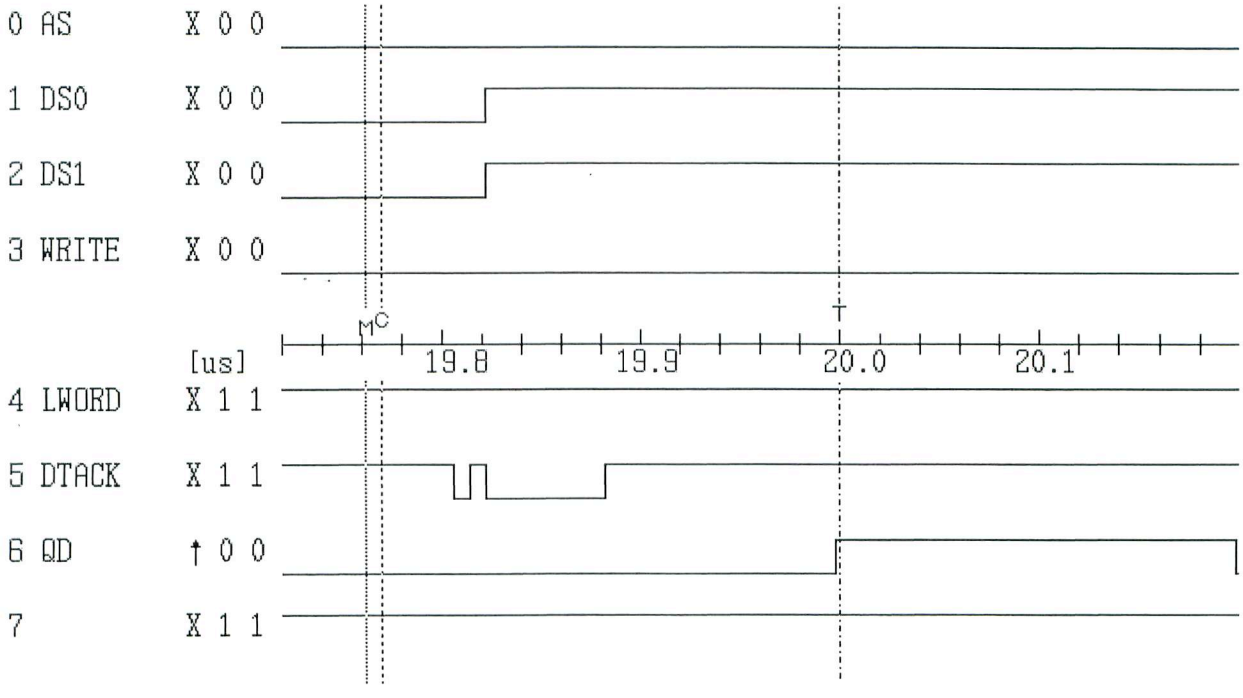


Fig. 4b. Abnormal wave form captured by a logic analyzer.

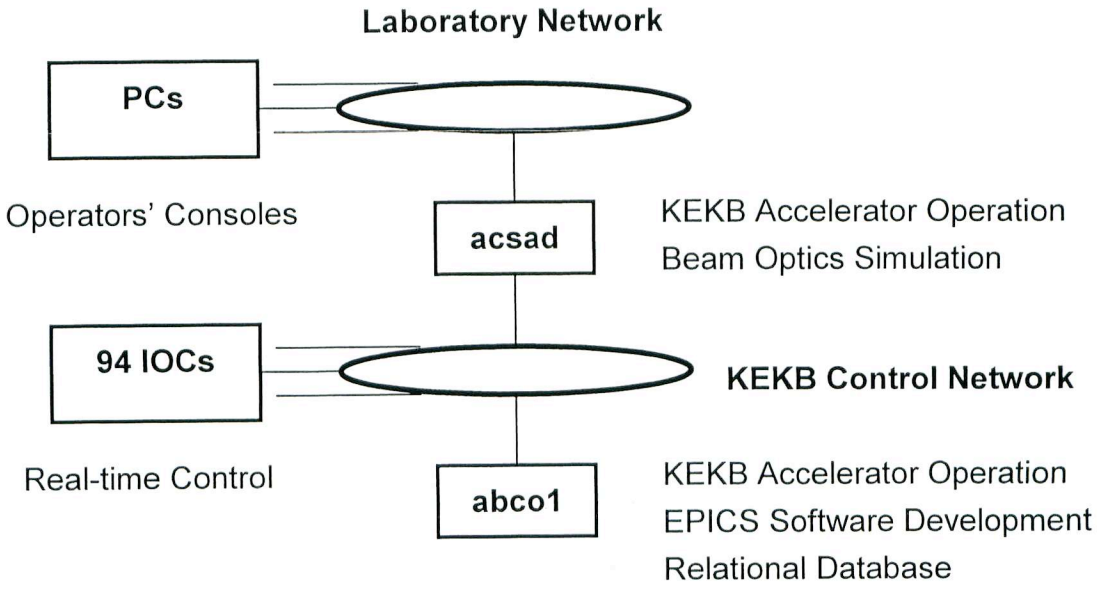


Fig. 5a. Schematic Diagram of Present KEKB Accelerator Control Computer System

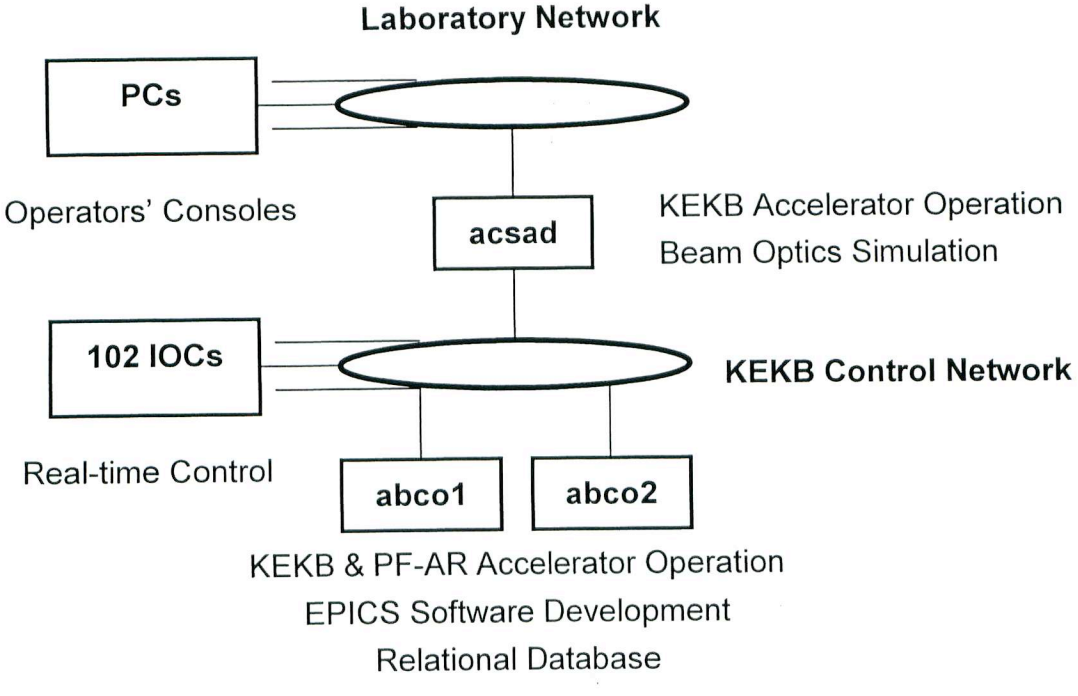


Fig. 5b. Schematic Diagram of KEKB/PF-AR Accelerator Control Computer System

KEKB Controls

KEKB Controls Group

Tadahiko Katoh

February 24, 2001

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- Works done since last Accelerator Review
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  2. Configuration Change of **acsad** Server Workstation
  3. Survey of Hardware Errors occurred in the BPM IOCs
- Work planned for the next one year
  1. PF-AR Accelerator Control System
  2. Console Desks in the Central Control Room

Application Software for Commissioning and Operations

- Application Programs written for KEKB Accelerator Commissioning and Operations

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◆ acsad4	V.5.1	57.7	27.3	3
◆ ~~*Total*~~		~~*328.3*~~	~~*209.5*~~	
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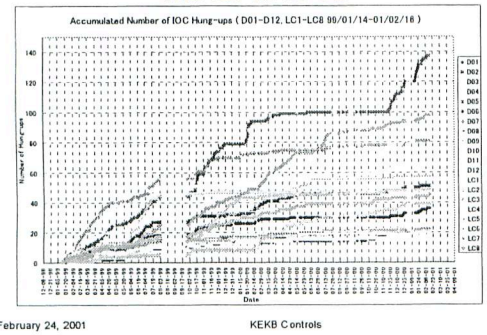
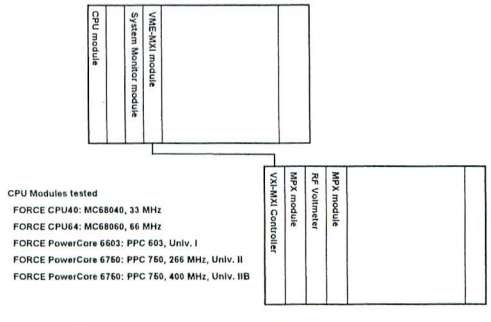
Survey of Hardware Errors Occurred in the BPM IOCs



Configuration of the Test Bench



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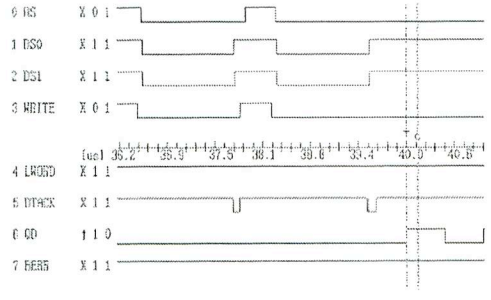
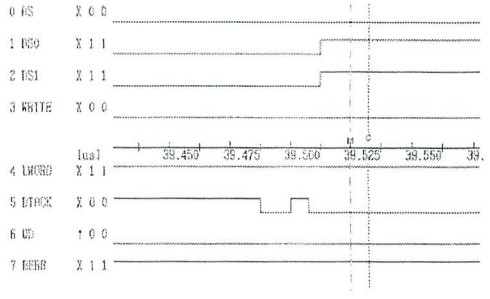
Normal and Abnormal Bus Cycles

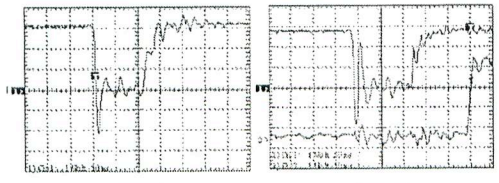


Abnormal Bus Cycle



Normal and Abnormal DTACK* Signals

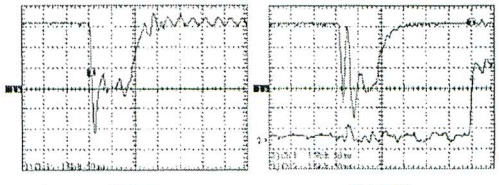
PowerCore 6603, with Universe I Chip



Normal Abnormal

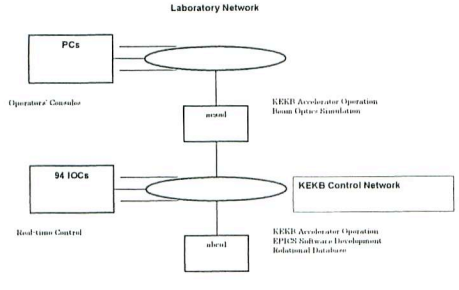
Abnormal DTACK* Signal

PowerCore 6750, 266 MHz, with Universe II



Normal Abnormal

Present KEKB Control System



KEKB/PF-AR Control System