Bunch Feedback Systems

KEKB Review, Feb. 10-11, 2003

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Present Status

Troubles since last MAC

- LER transverse feedback kicker broken
- High power attenuator burned
- High power wideband amplifies broken

Development of the Next Generation Digital Filter Systems for SuperKEKB/SuperPEP-II/Light sources.

Present status

Without transverse feedback systems

- Strong horizontal and vertical instabilities appears
- HER <40mA, LER <60mA (horizontal)

With transverse feedback

- Single beam : HER >850mA, LER >1400mA
- Colliding mode : ~1000mA(HER) ×1600mA(LER)

Feedback related systems

- Bunch current monitors
- Betatron tune measurement systems(global & gated)
- Bunch oscillation monitor systems with beam loss trigger
  - also working very well! (by Fukuma)

Heating of vacuum components for feedback systems

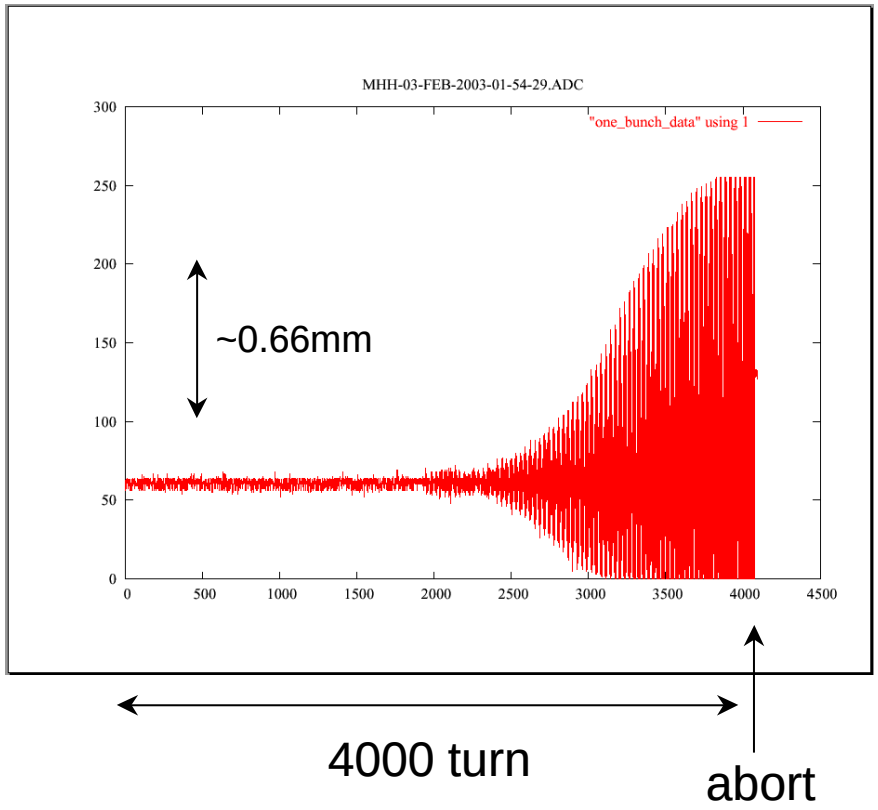
- Marginal up to present maximum current (~1600mA)

Bunch Oscillation Recorder (BOR)

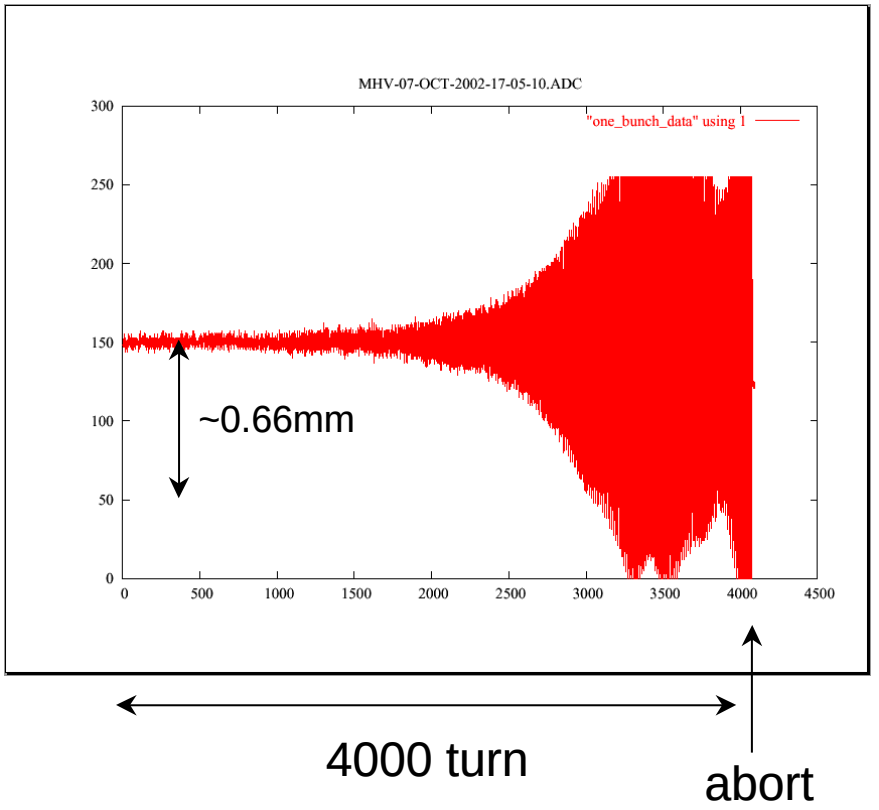
Very useful for abort and instability diagnostics

Examples of HER beam oscillation at beam abort

(horizontal)



(vertical)



Troubles

Breakdown of LER transverse kicker(Mar/2002)

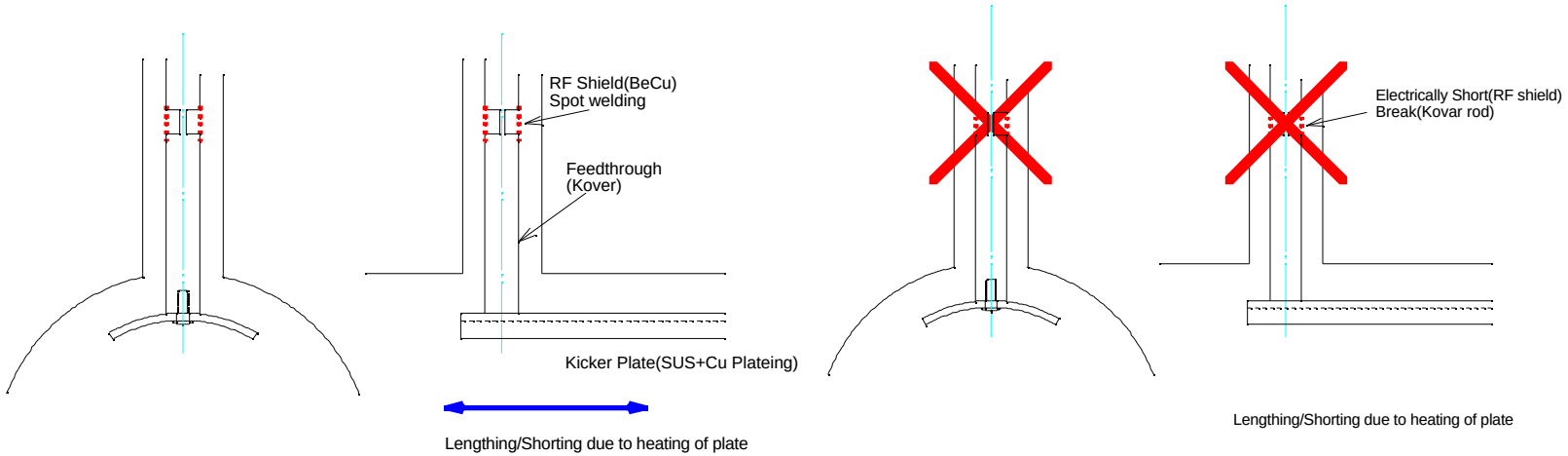
Direct cause: use of incorrect screws to tie kicker plate to feedthrough.

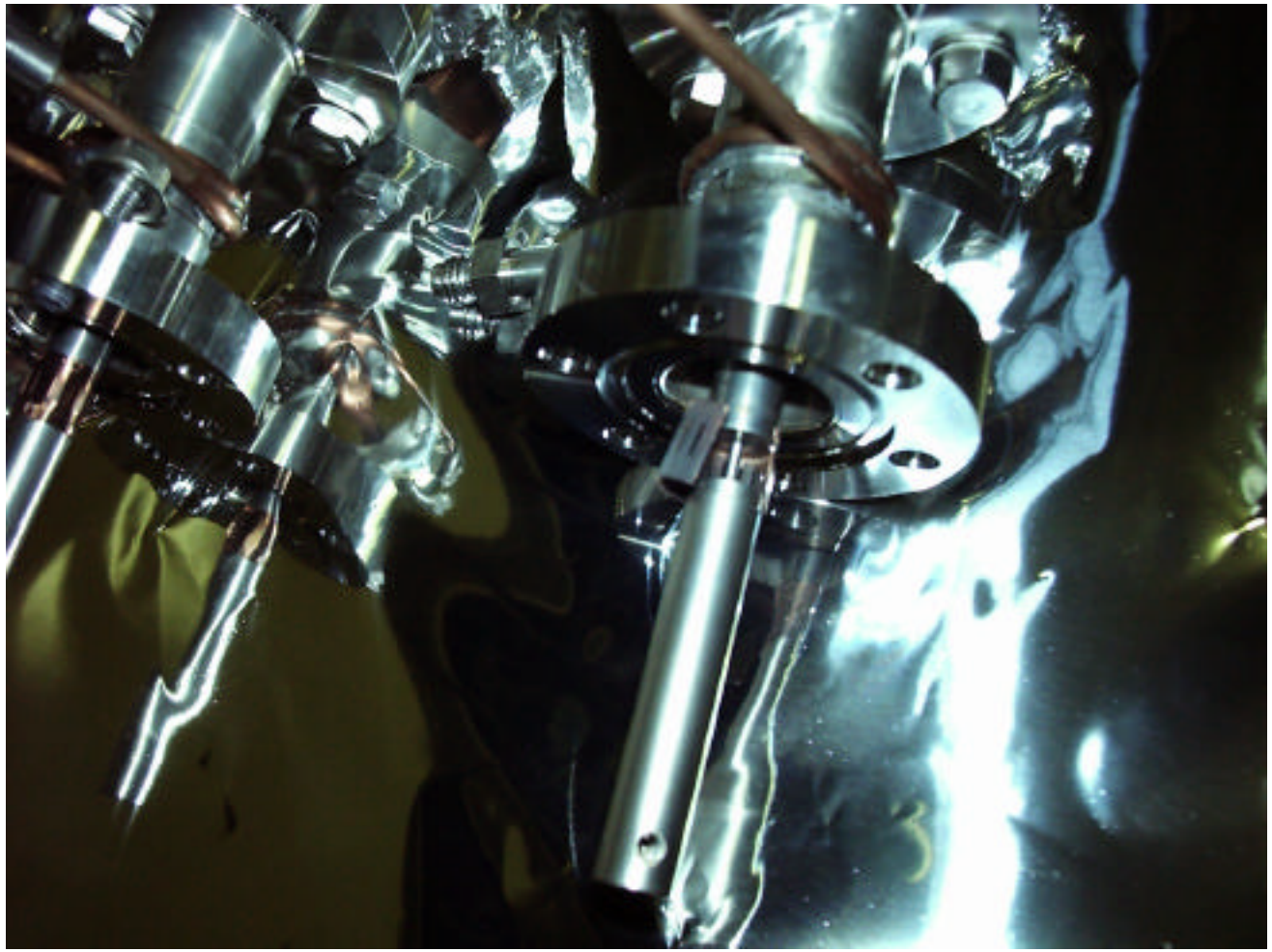
Moreover…

Improper mechanism to cure lengthening of kicker plates.

History of troubles of kicker feedthroughs.

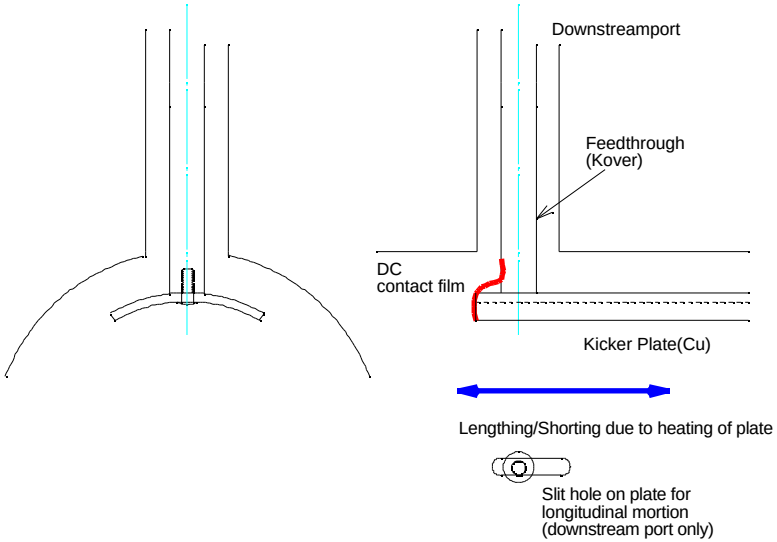
[1] Up to Summer 2001

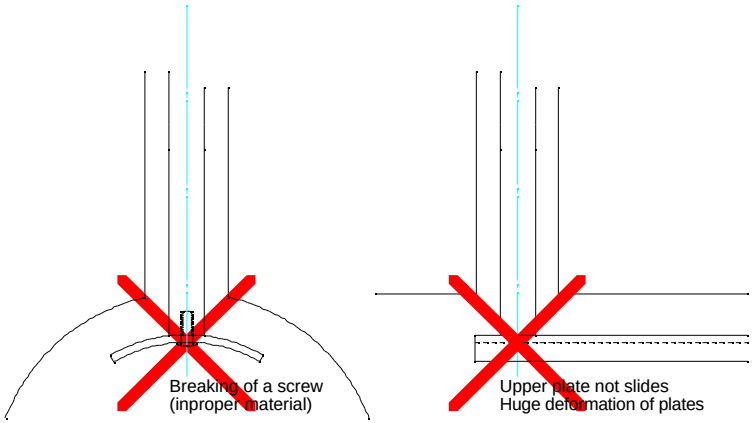




[2] Summer 2001 - Summer 2002

Second type (Fixed feedthrough + slide mechanism on plate)





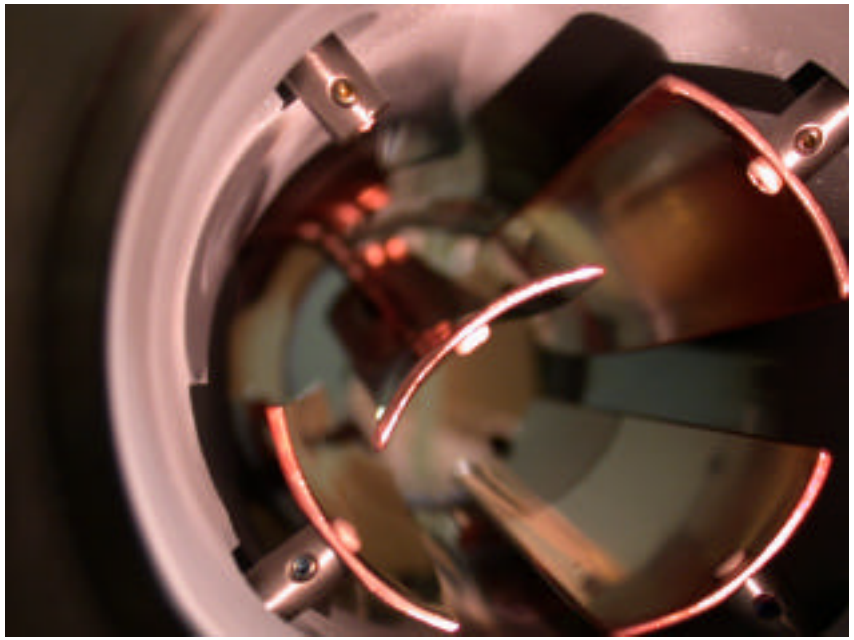
Ohmic loss of beam induced current at I_b~1400mA

Cu plate ~0.93W

Kover rod ~1.2W

→ $\Delta T<150$deg, $\Delta L<1$mm: tolerable

LER Kicker breakdown on 10/Mar/2002

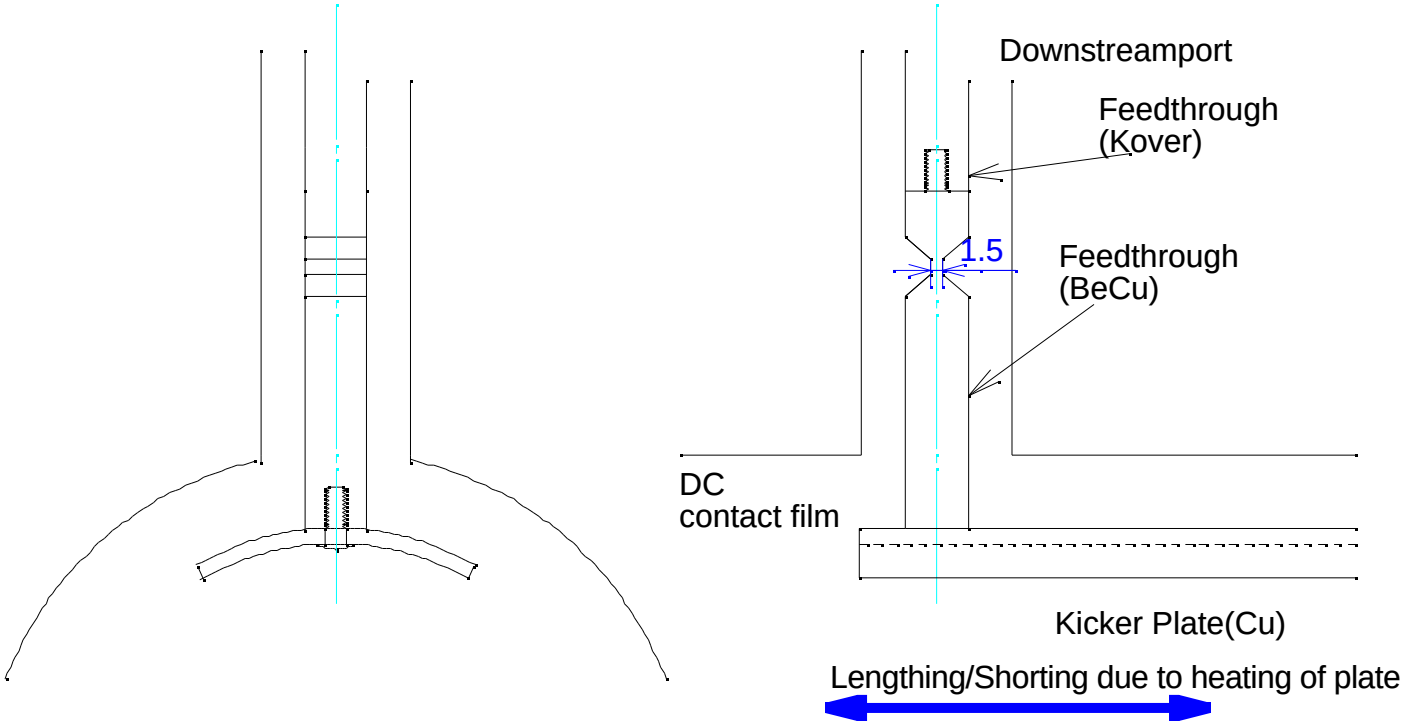


[3] From Summer 2002

Third type (present feedthroghs for both HER/LER)

BeCu spring rod : downstream(rf power ampl. side) only

No resonance on the neck structure up to ~4GHz by HFSS



Burnout of a high-power attenuator for the LER transverse kicker

N-connectors of the attenuator and the cable has been melted.

Add reflection power alarm.

Two high-power amplifiers has damaged (LER 1/ HER 1)

LER : one final FET chips broken

HER: Power supply problem (trouble in SW PS)

Development of the Next Generation Digital Filter Systems for SuperKEKB / SuperPEP-II / Light sources.

International Collaboration

SLAC (J. Fox, D. Teytelman, L. Beckman, M. Tobiyama)

KEKB (M.Tobiyama + feedback/monitor group)

+ DAFNE, ALS, APS, BESSY-II, etc..

*Letter of intent to SLAC by J. Fox; dated 1-28-03

GBoard Processing Channel project proposal

Design/simulation on FPGA and ultra fast logic system is underway since Jun/2002 and critical high-speed signal processing channel has been verified via functional and timing verification up to now.

Remaining tasks - the real detailed engineering.

Digital filter system for bunch by bunch feedback systems

PEP-II

DSP based digital feedback system (downsampled).

Longitudinal only

Completely programmable and flexible.

ALS, DAΦNE,PLS,BESSY-II,

SPEAR…

KEKB

Hardware two-tap FIR filter system non-downsampling

with custom MPX/DMPX ICs

Transverse & Longitudinal

Very limited flexibility

KEKB only

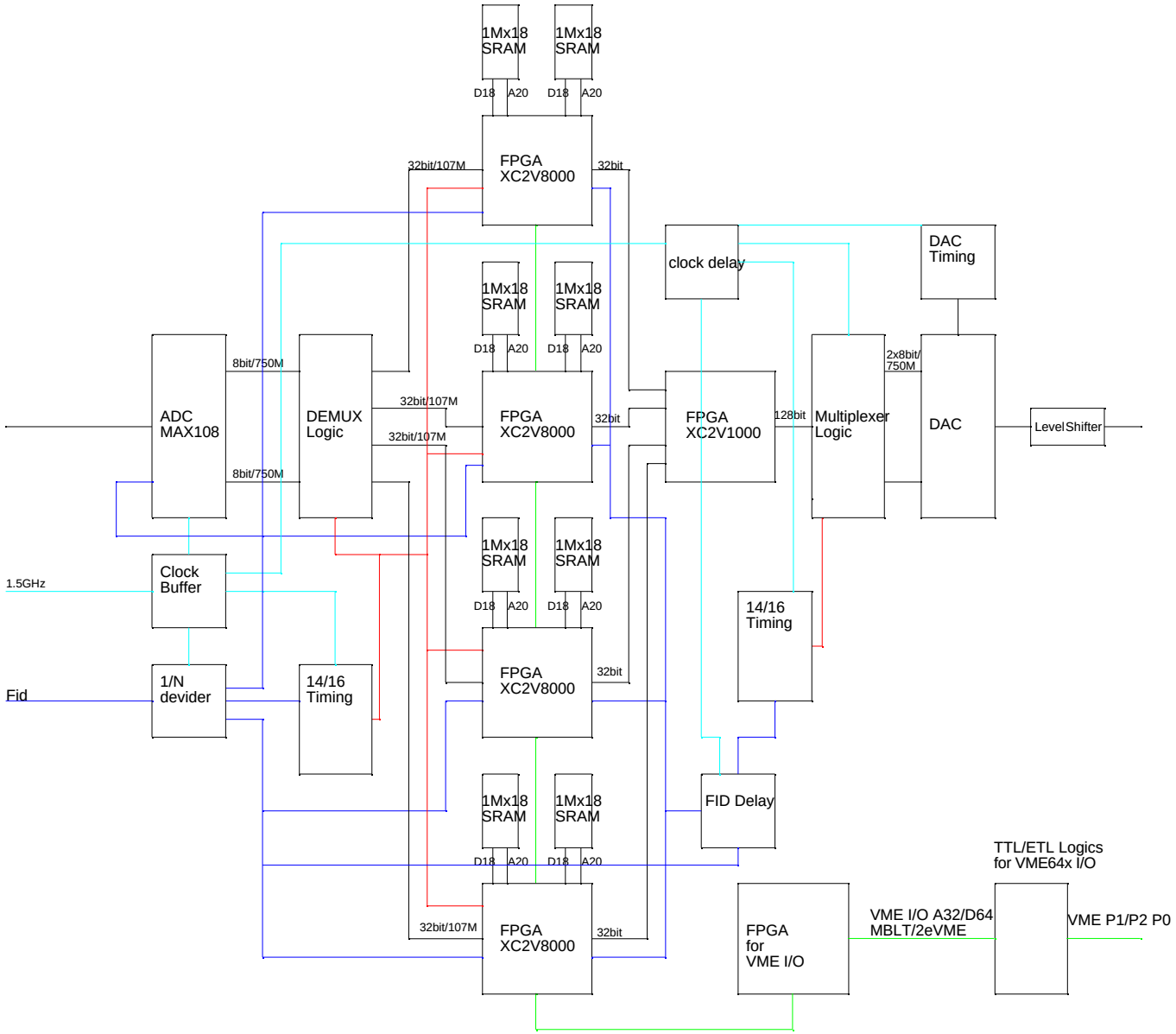
Very high-speed FPGA(ex. Vertex-II) with huge logic space and enough memory space available.

High-speed ADC (1.5GSPS), Logic chips (>3GHz) available.

Very dense SRAM available

Specifications

- Support bunch spacing down to 0.66 ns - sampling at 1.5 GHz.
- Support quasi-arbitrary harmonic numbers.
- Independent processing for all bunches on all turns - required for transverse feedback.
- Diagnostic memory capable of holding 20 ms of data at the full rate
- Support downsampled processing - reuse the hardware to get longer filters
- Support downsampling for diagnostics for studying slow events
- Support long FIR or IIR filters


1Mx18 SRAM
1Mx18 SRAM
D18
A20
D18
A20
FPGA XC2V8000
32bit/107M
32bit
clock delay
DAC Timing
1Mx18 SRAM
1Mx18 SRAM
D18
A20
D18
A20
2x8bit/ 750M
ADC MAX108
8bit/750M
DEMUX Logic
32bit/107M
32bit/107M
FPGA XC2V8000
32bit
FPGA XC2V1000
128bit
Multiplexer Logic
DAC
Level Shifter
8bit/750M
1Mx18 SRAM
1Mx18 SRAM
D18
A20
D18
A20
1.5GHz
Clock Buffer
14/16 Timing
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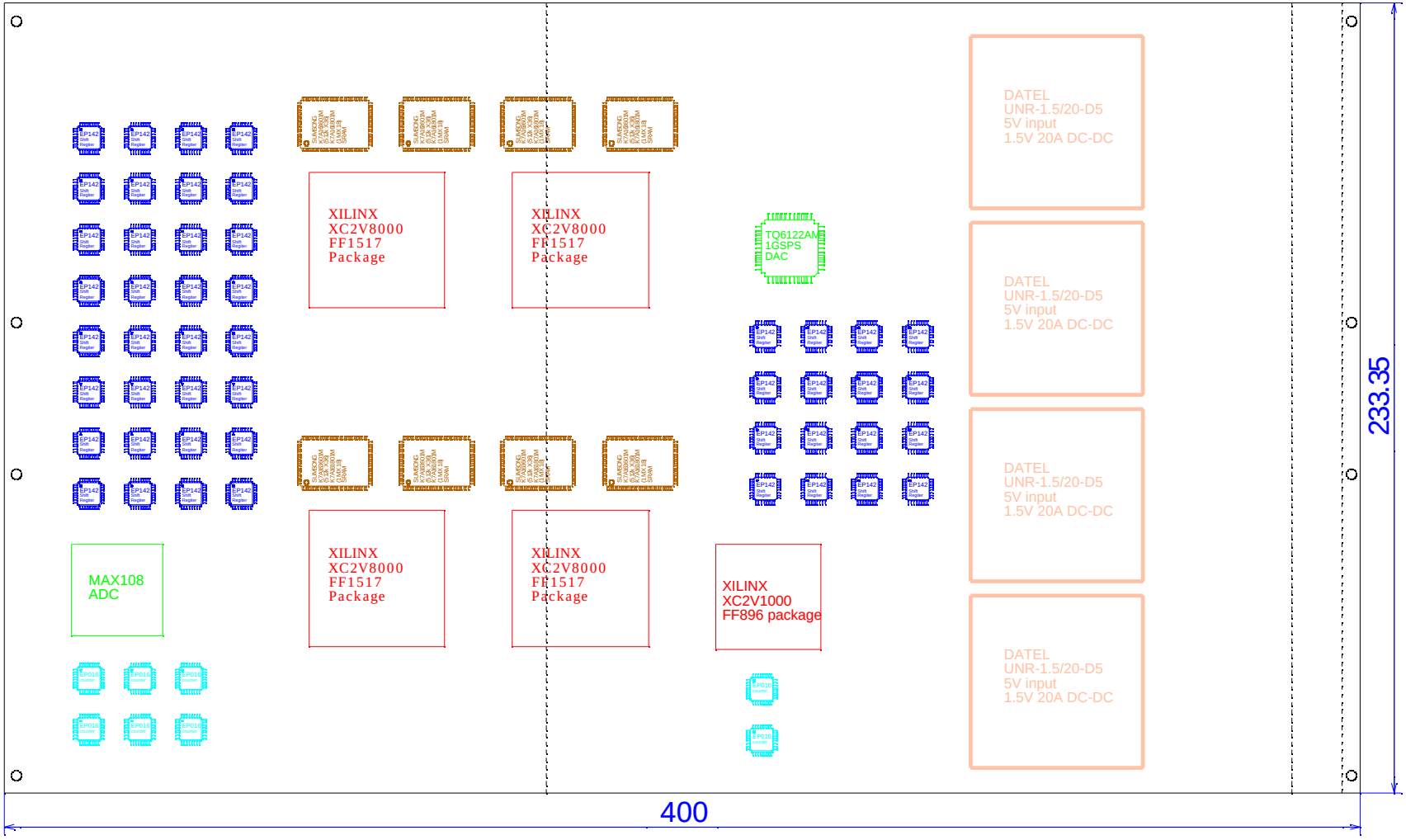
14/16 Timing
FPGA XC2V8000
32bit
1Mx18 SRAM
1Mx18 SRAM
FID Delay
D18
A20
D18
A20
TTL/ETL Logics for VME64x I/O
32bit/107M
FPGA XC2V8000
32bit
FPGA for VME I/O
VME I/O A32/D64 MBLT/2eVME
VME P1/P2 P0


XILINX
XC2V8000
FF1517
Package
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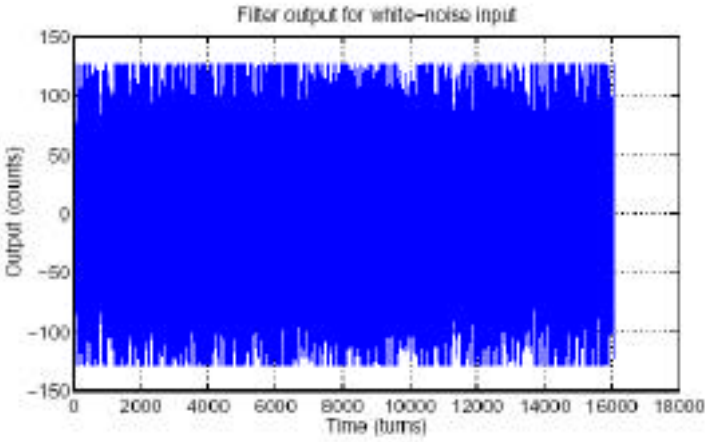
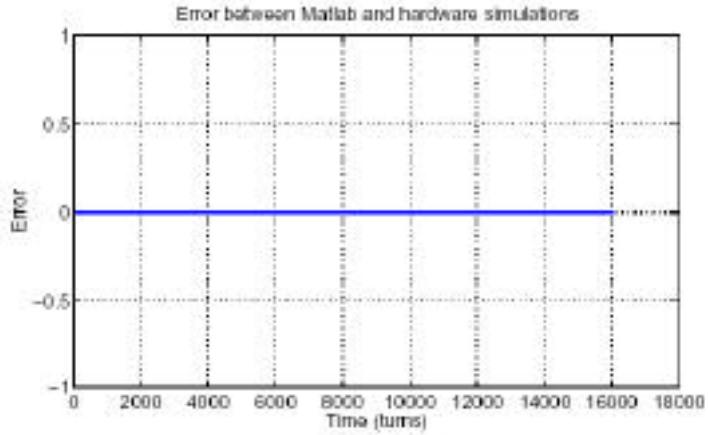
XILINX
XC2V8000
FF1517
Package
TQ6122AM
1GSPS
DAC
MAX108
ADC
XILINX
XC2V1000
FF896 package
DATEL
UNR-1.5/20-D5
5V input
1.5V 20A DC-DC
DATEL
UNR-1.5/20-D5
5V input
1.5V 20A DC-DC
DATEL
UNR-1.5/20-D5
5V input
1.5V 20A DC-DC
DATEL
UNR-1.5/20-D5
5V input
1.5V 20A DC-DC
233.35
400

Functional simulation of a 20-tap FIR channel

A 20-tap FIR channel was designed for the FPGA implementation.

- 8 bit ADC data
- 8 bit DAC output
- 16 bit coefficients
- Full width accumulators (24-29 bits)
- Shift gain of 0-7 bits
- Output saturation to 8 bits
- FPGA resource usage - 13%
- Compiled implementation has 6.3 ns cycle time - for 1.5 GHz we need 9.3 ns.
- Functional simulation (Innoveda Fusion) for 8 groups (DAΦNE case) using white noise input signal
- Compared to bit-true MATLAB simulation





Schedule

Jun/02 – Apr/03	Design of FPGA/Fast Logic/Interface
May/03 - Aug/03	Detailed engineering design for prototype
Aug/03 - Mar/04	Fabrication of 1st prototype board
	Test & feedback to next prototype..

Estimated cost

FY2003	PCB board design	$30k
	Prototype board fablication	$75k
	Test station	$25k
	Lab test equipments	$30k
	Total $160k + travel cost	$30k

About $100k/year for design/fablications (roughly 3 years)

until final version board	+$200,000
Production cost for final board	$20,000/board
Travel expenses	?

International collaboration between SLAC/PEP-II and KEK/KEKB.