

Development of New LLRF System

~ KEKB LLRF Team ~

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Talk Outline

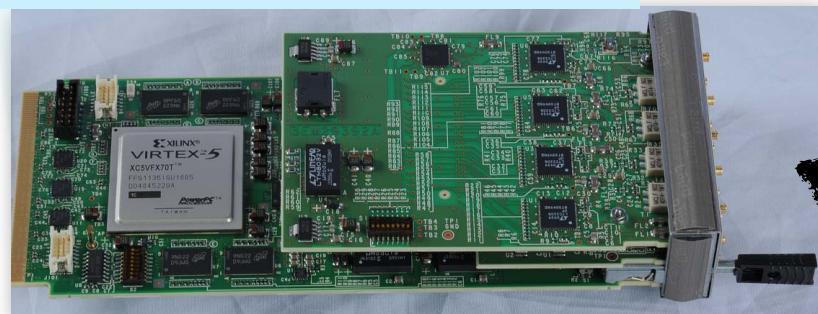
- 1. Overview the Digital LLRF System**
- 2. Performance Evaluation of the prototype**
 - a) FB Control**
 - b) Temperature Dependency**
 - c) Auto Tuner Control**
- 3. RF Reference Distribution**
- 4. Summary**

Features of New LLRF System

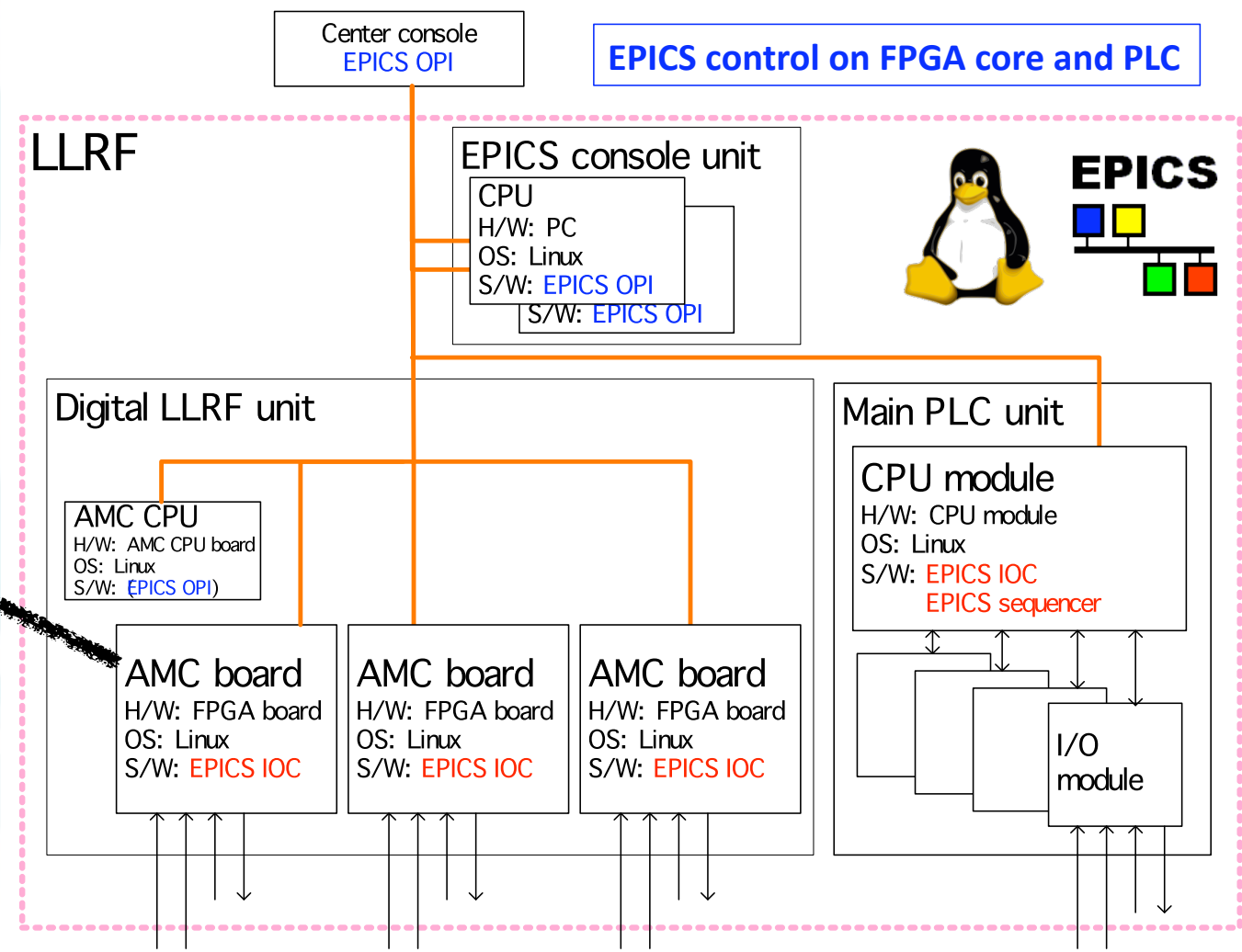
Preset analog systems will be replaced by new digital ones step-by-step.

- It consists of μ TCA-based FPGA boards & PLC (EPICS-Sequencer).
- EPICS-IOC on Linux-OS is embedded in each of them. They can be operated remotely via EPICS-Channel Access.
- Hardware is common for both of ARES & SC Cavity. (Also both softwares are much the same.)
- EPICS record names will be consistence with the present systems.
- Klystrons (LLRF) : Cavity unit = 1 : 1 (SuperKEKB)

uTCA-platform
FPGA Boards



with CPU (PPC) running
Linux-OS for EPICS-IOC.



Prototype of New LLRF System

for the SuperKEKB

A prototype of new digital LLRF system (α -version) was produced in last year. And the performance was evaluated.

New LLRF System for one klystron (EIA-19" rack)

PLC : EPICS Sequencer (F3RP61)

RF-Output Unit (IQ-Modulator & RF-SW)

μ TCA-based Digital FB unit

Down Converter Unit (IF out)

RF Interlock Unit

Distribution Unit (LO & CLK generation and distribution)

Linux-OS PC's with EPICS

Operate via CA

GUI is composed by using EDM.

Arc Sensor

μ TCA

uTCA-platform Digital Control Unit

common with the STF.

PM (Power Module)

AC/DC

MCH

CPU

HDD

Board - (A)

MMC-DFB02-B

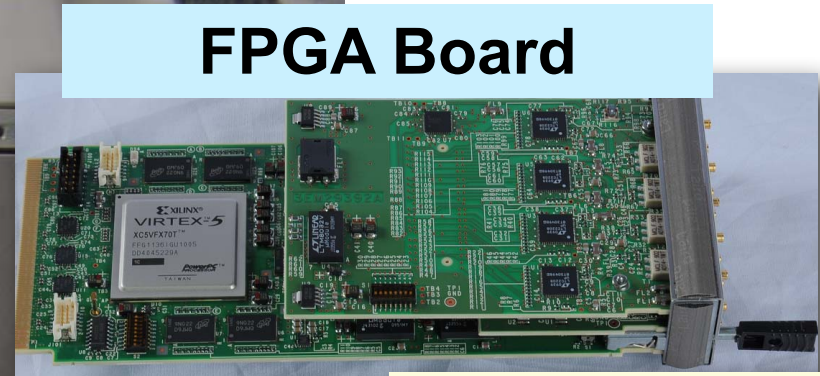
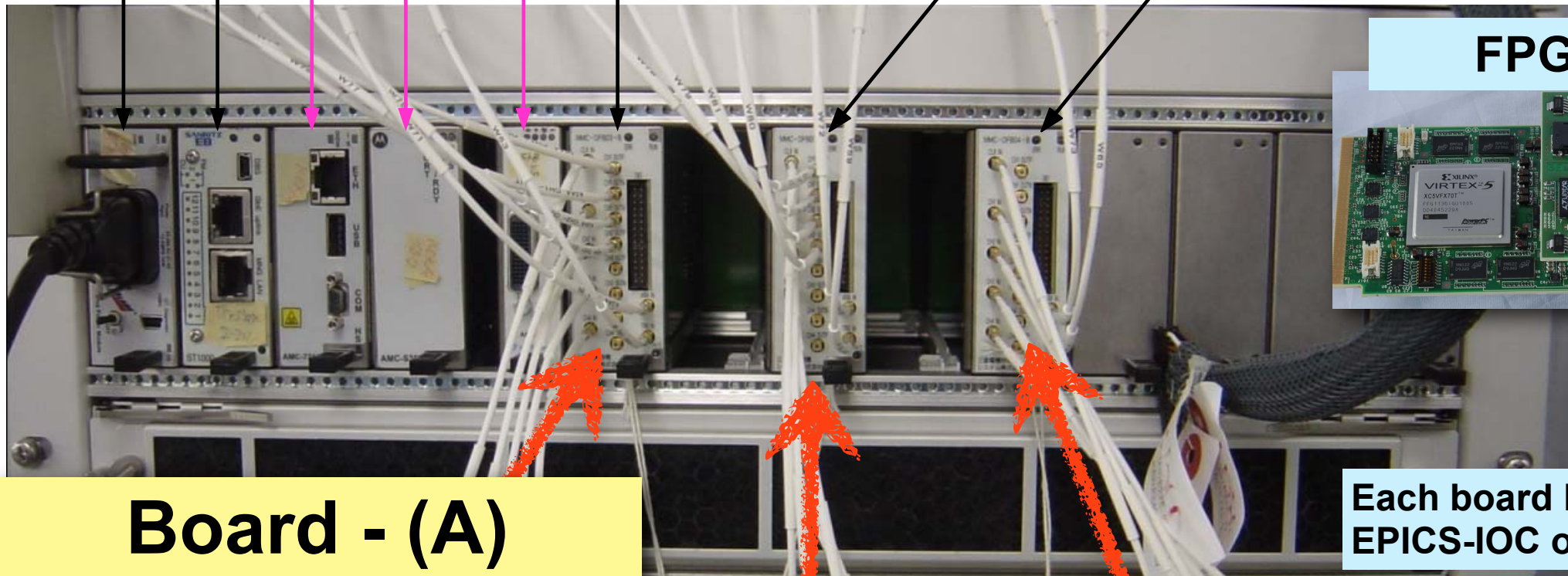
DVI

Board - (B)

MMC-DFB03-B

Board - (C)

MMC-MON02-B



FPGA Board

16-bit ADC x 4ch,
16-bit DAC x 2ch

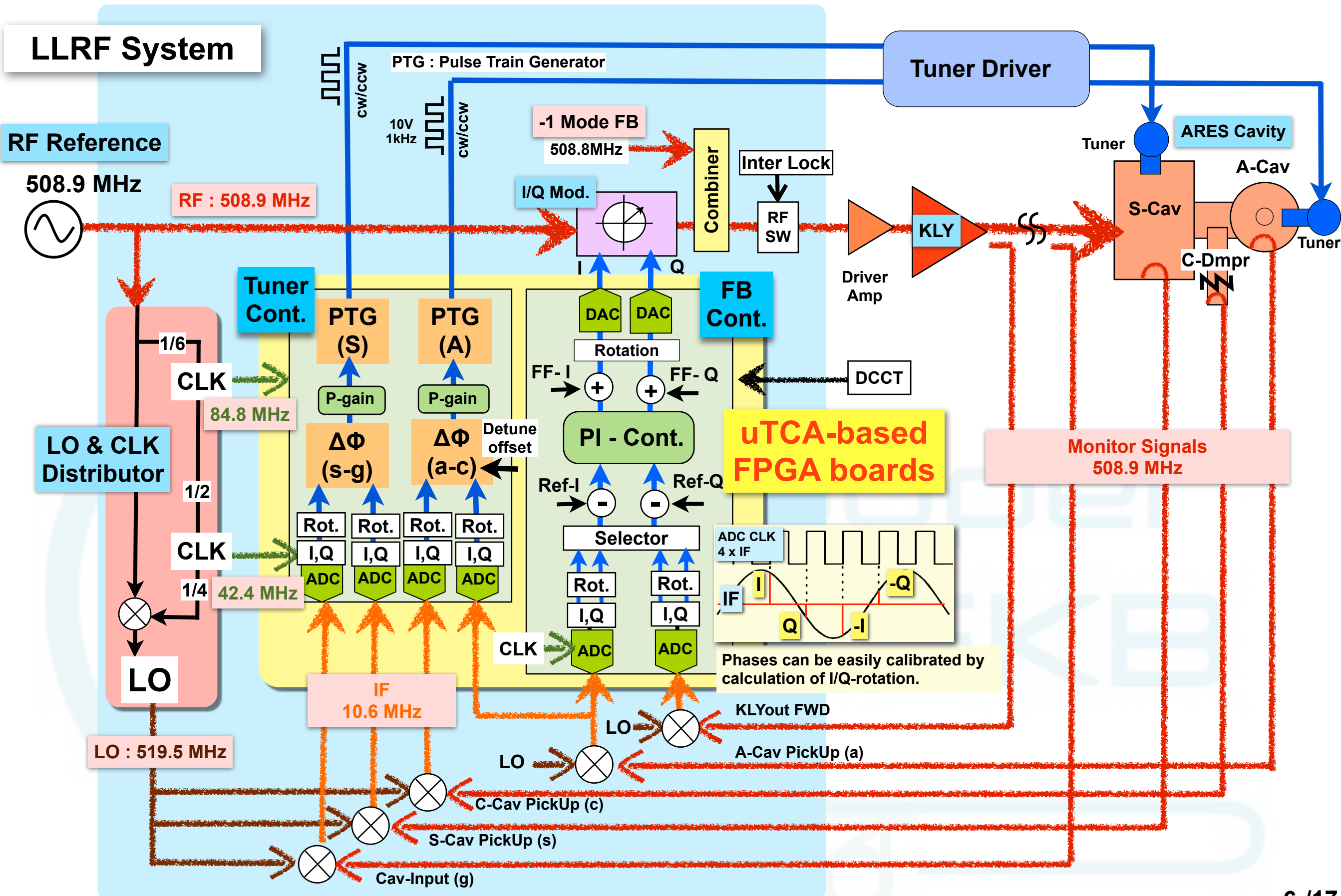
Each board has a CPU (PPC), and the EPICS-IOC on Linux-OS is embedded.

**Board - (A)
Digital FB Control**

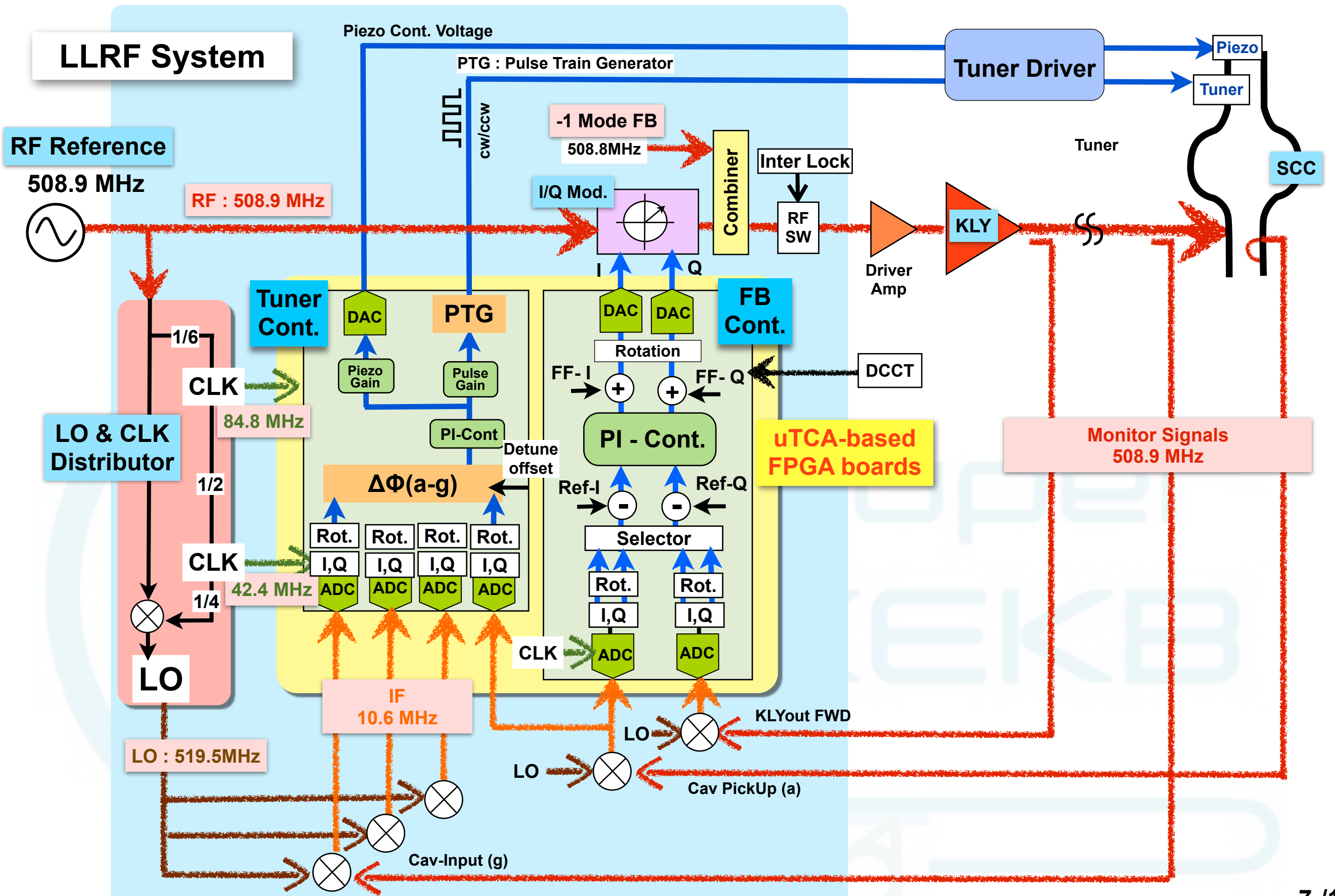
**Board - (B)
Tuner Control**

**Board - (C)
I/L Control
& VSWR Monitor**

Block Diagram of FB&Tuner Cont. (ARES)

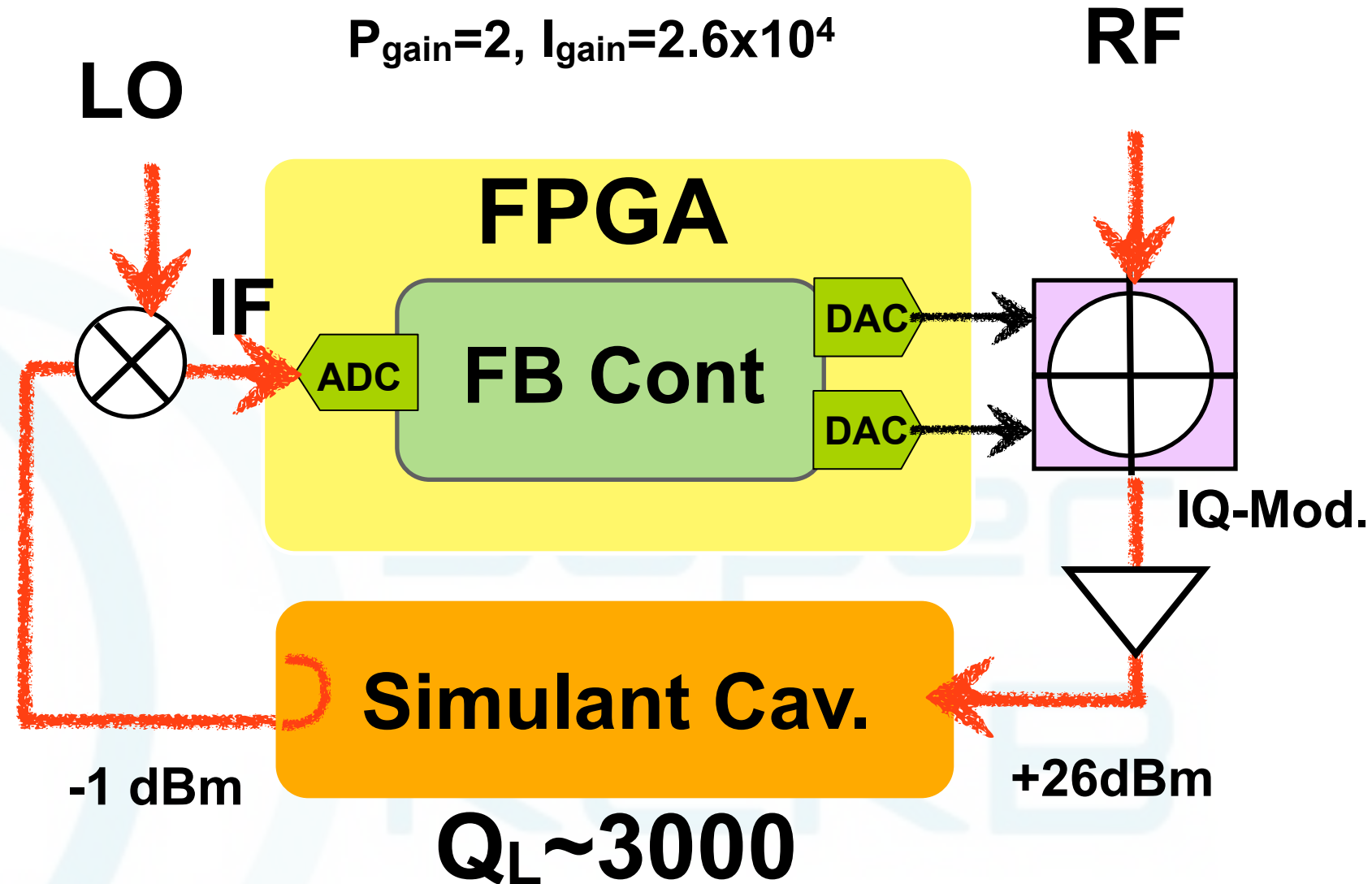
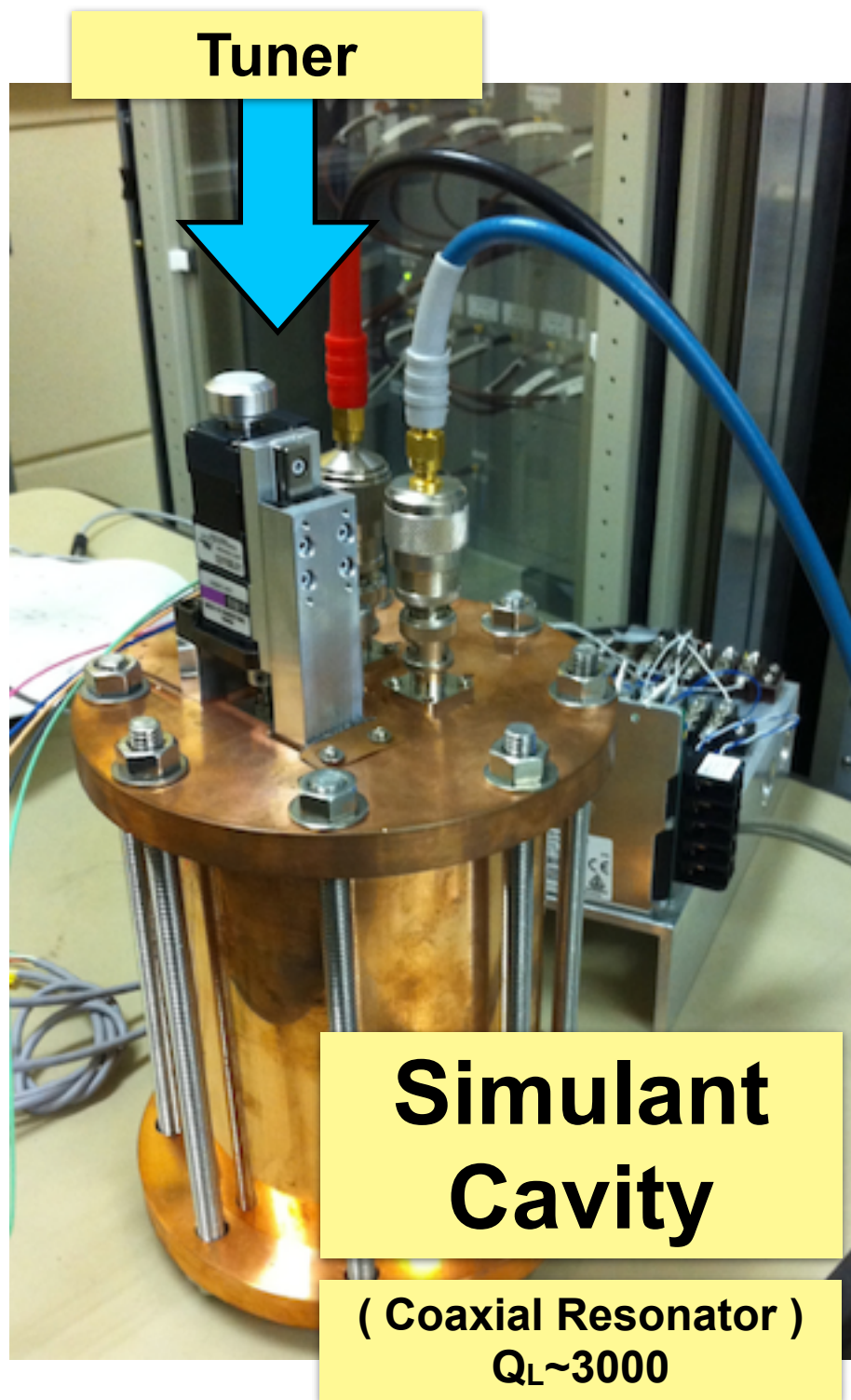


Block Diagram of FB&Tuner Cont. (SC)



Evaluation of FB Control

FB control performance was evaluated by using a simulant cavity



This evaluation condition is more adverse than the real operation for the stability.

ARES Cavity: $Q_L \sim 20000$ ($\beta \sim 5$)

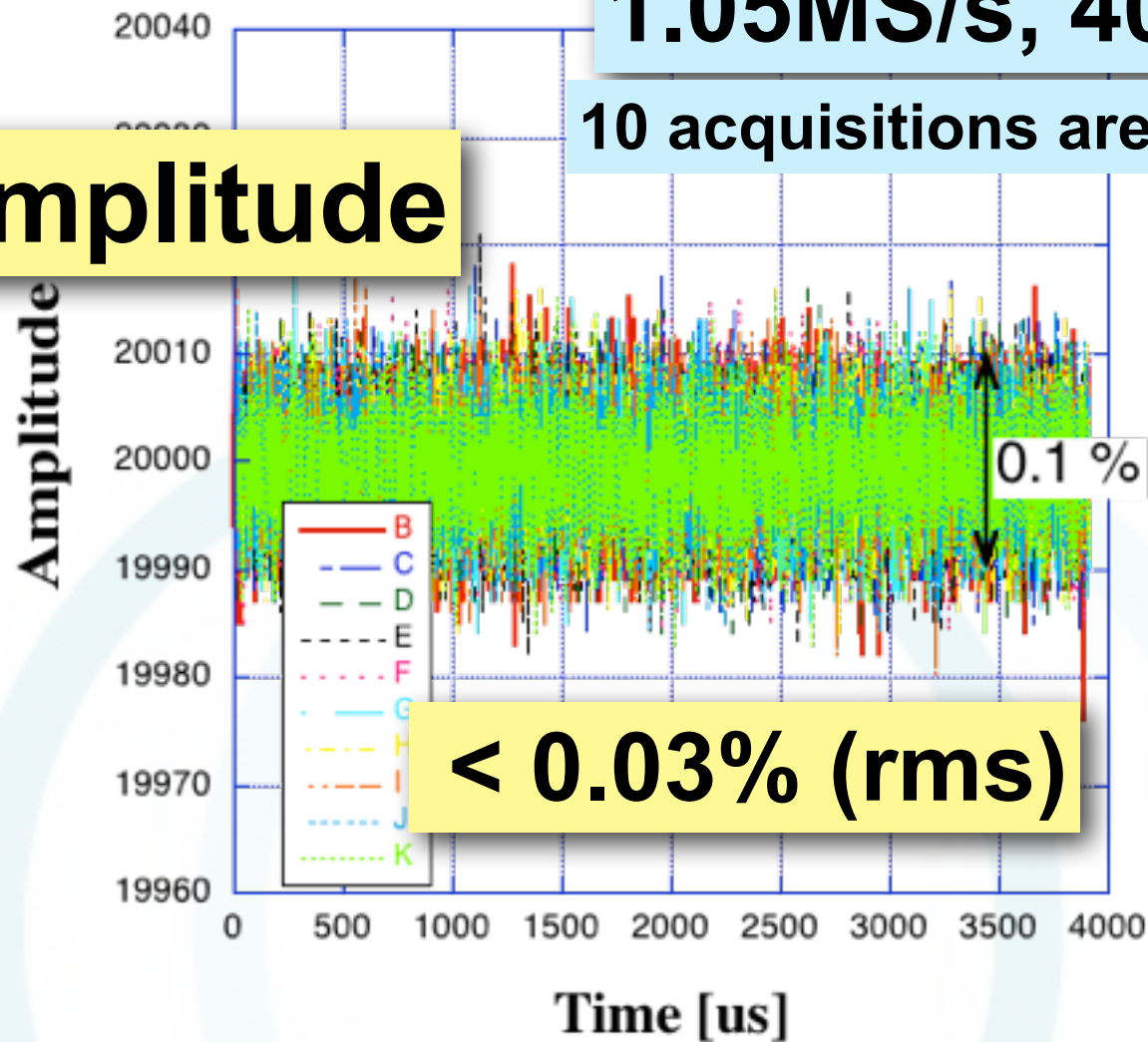
FB Control Result

(Monitored Data by FPGA acting FB cont.)

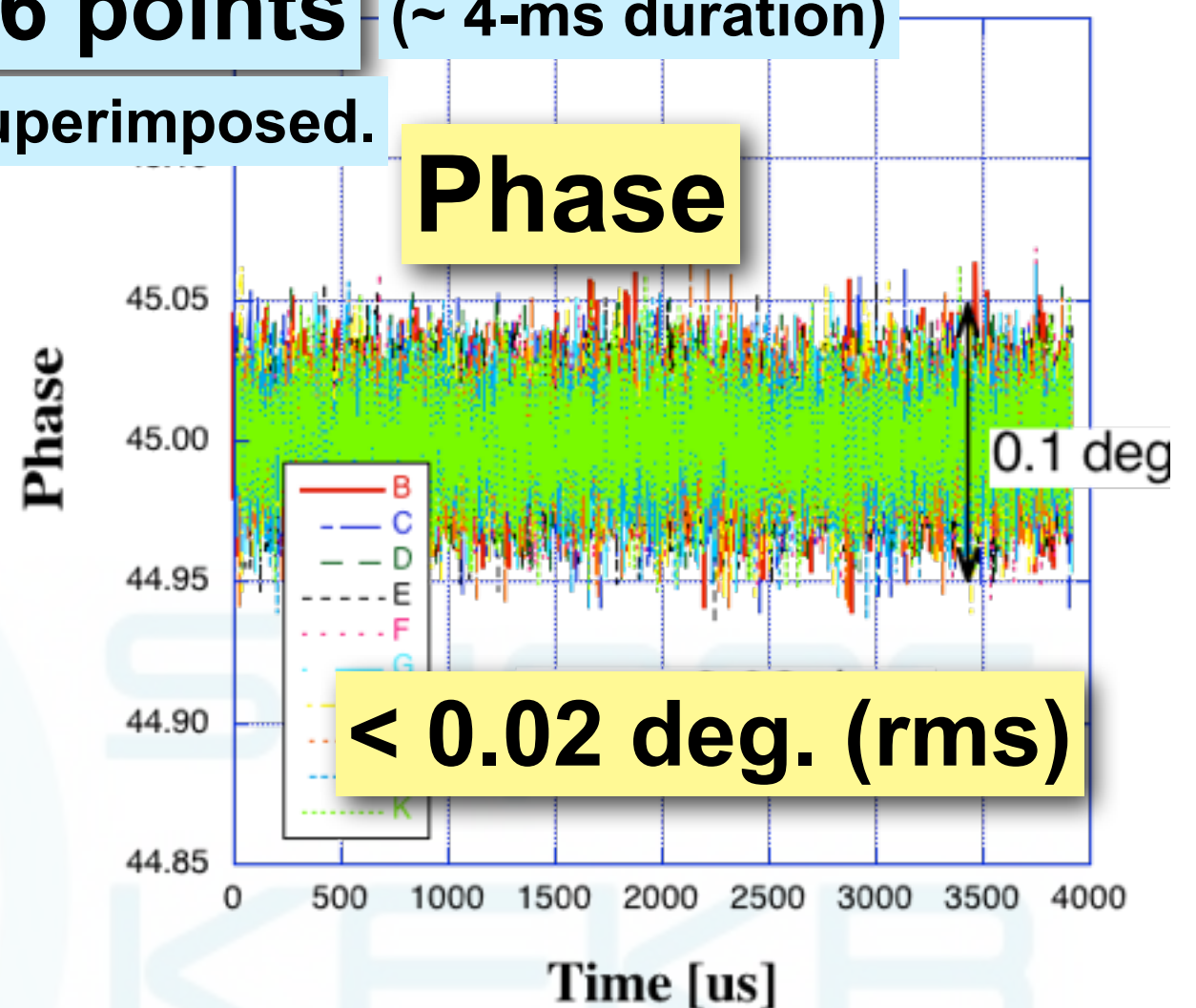
1.05MS/s, 4096 points (~ 4-ms duration)

10 acquisitions are superimposed.

Amplitude



Phase



Very good stability was obtained.

The amplitude and phase stabilities are 0.03% and 0.02 deg., respectively.

The FB control performance satisfy the requirements very well in short term stability.

Long Term Stability or Temperature Dependency

for acc. gradient

Required Stability

**+/- 1% in Amplitude
+/- 1 deg. in Phase**

Our target value of the stability

for LLRF System

**+/- 0.3% in Amplitude
+/- 0.3 deg. in Phase**

(pk-pk)

Ambient Temperature Change : about +/- 2 deg.C

**Acceptable
Temp. Coefficient**

**0.1%/deg.C in Amplitude
0.1 deg./deg.C in Phase**

Measured Result

LLRF system total

**Amplitude: 0.5 % / deg.C
Phase: 0.25 deg. / deg.C**

Requirements are not satisfied.

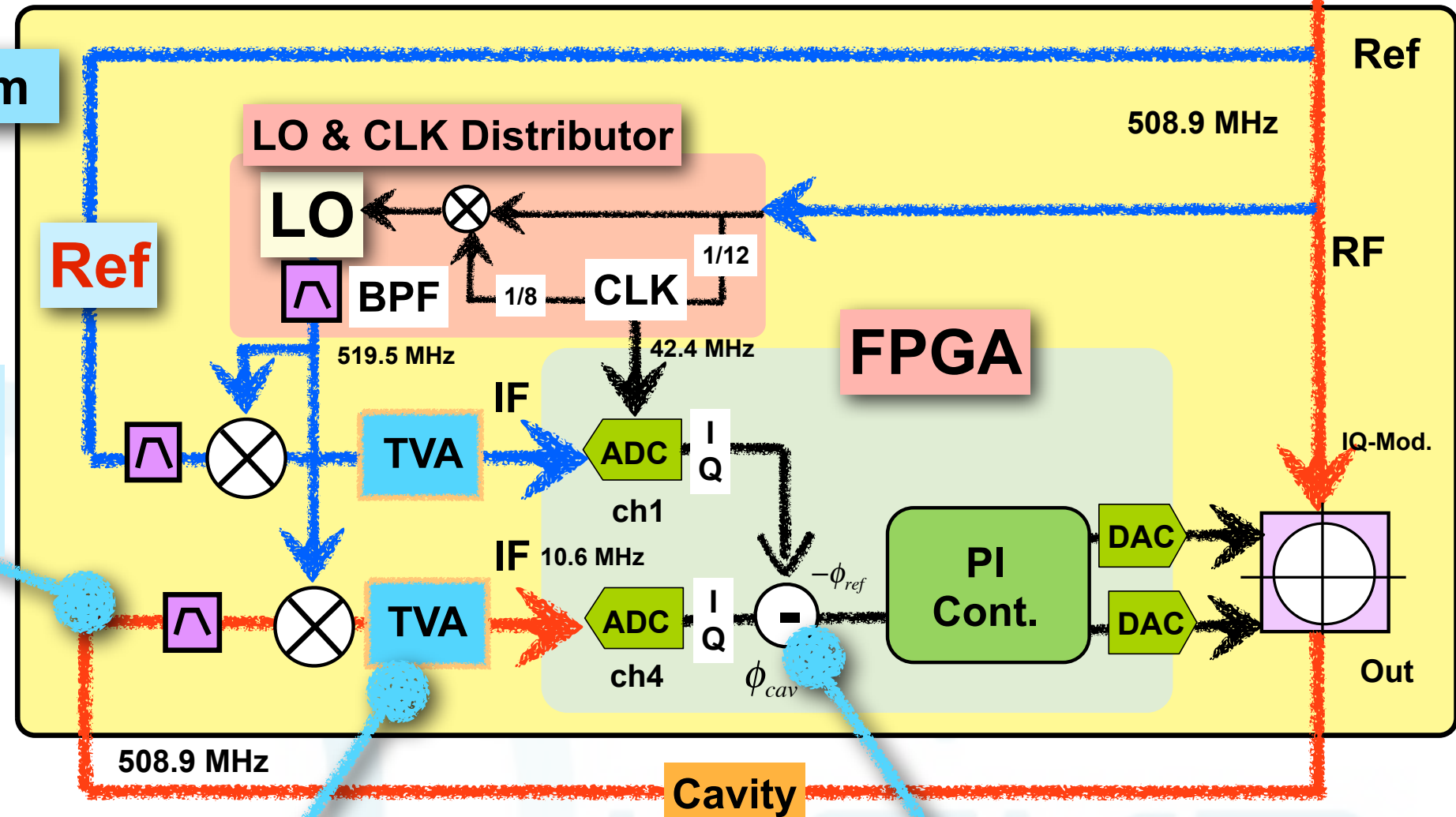
Countermeasure for Temperature Dependency

From the evaluation of each RF element device,
It was found that the **BPF** property is **main factor** for the temperature dependency.
However, **BPF is essential** in the LO generation and pick-up RF monitoring.



LLRF System

Appropriate BPF, of which **temperature coefficient** is **lower**, will be selected as much as possible.



“Thermal Variable Attenuators (TVA)” will be inserted here to compensate amplitude change.

For the phase stability, Directly reference signal is monitored together on FPGA, and the FB-control will be calibrated with the reference.

Amplitude

0.09 % / deg.C

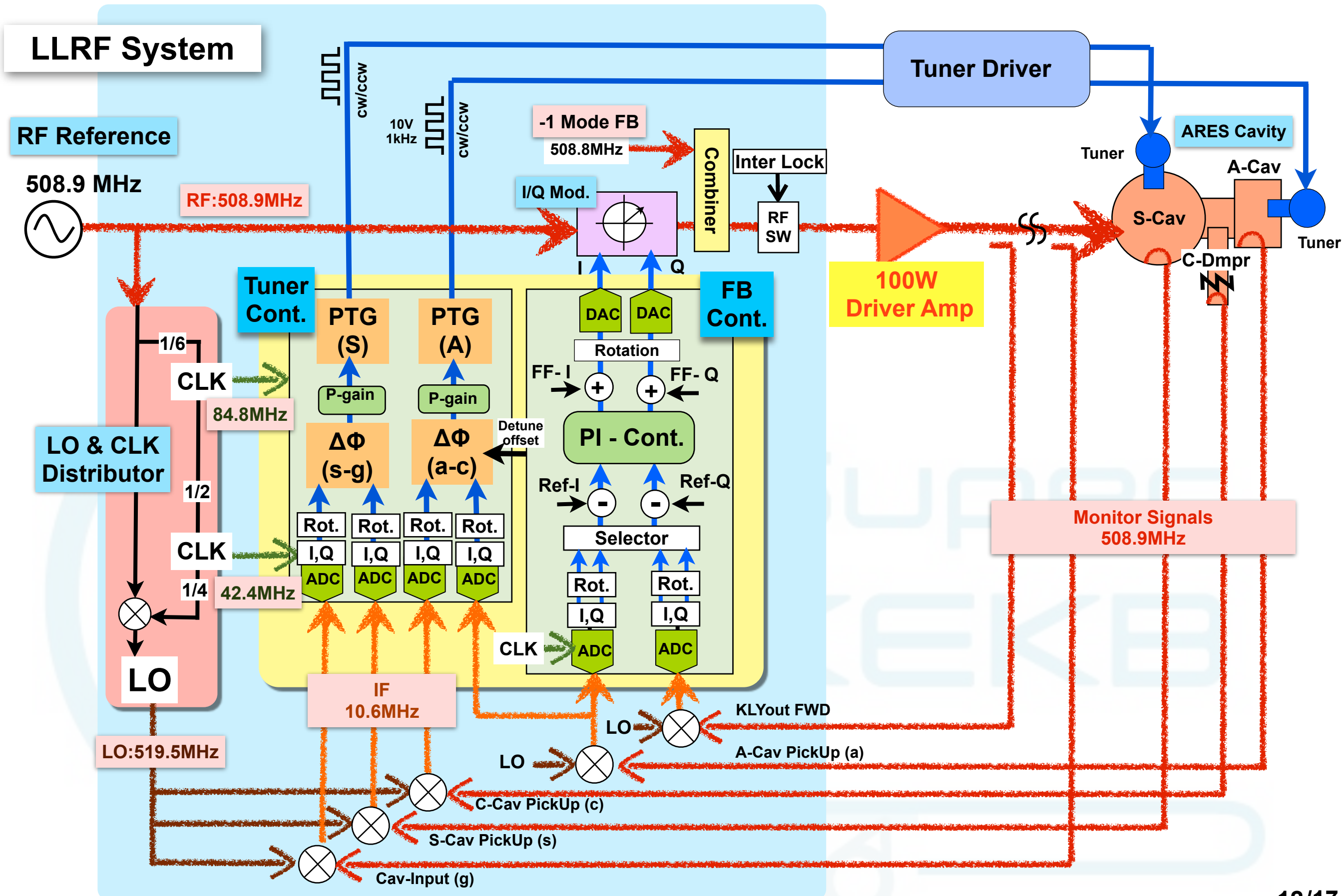
Phase

0.04 deg. / deg.C

Expected Value

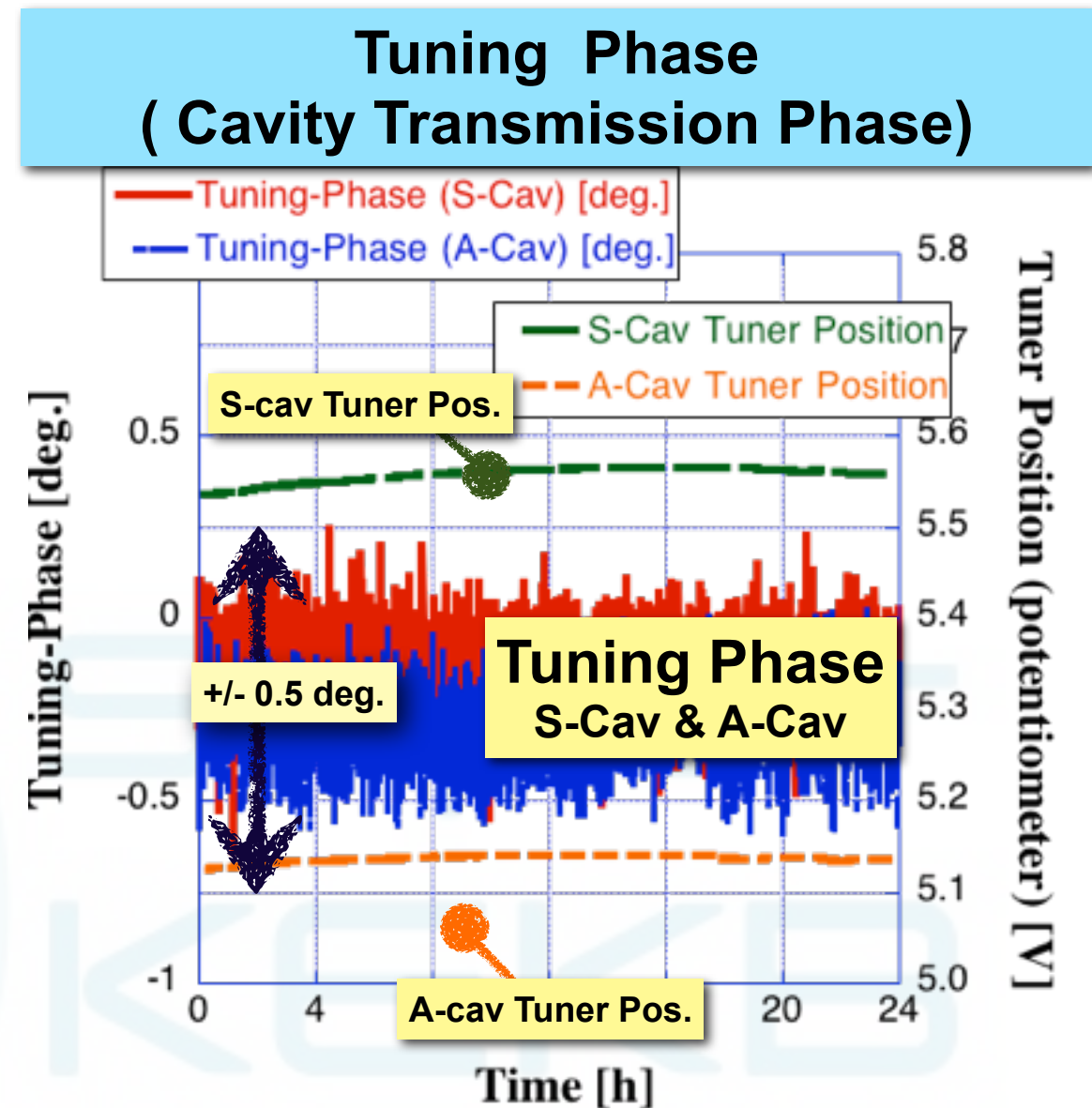
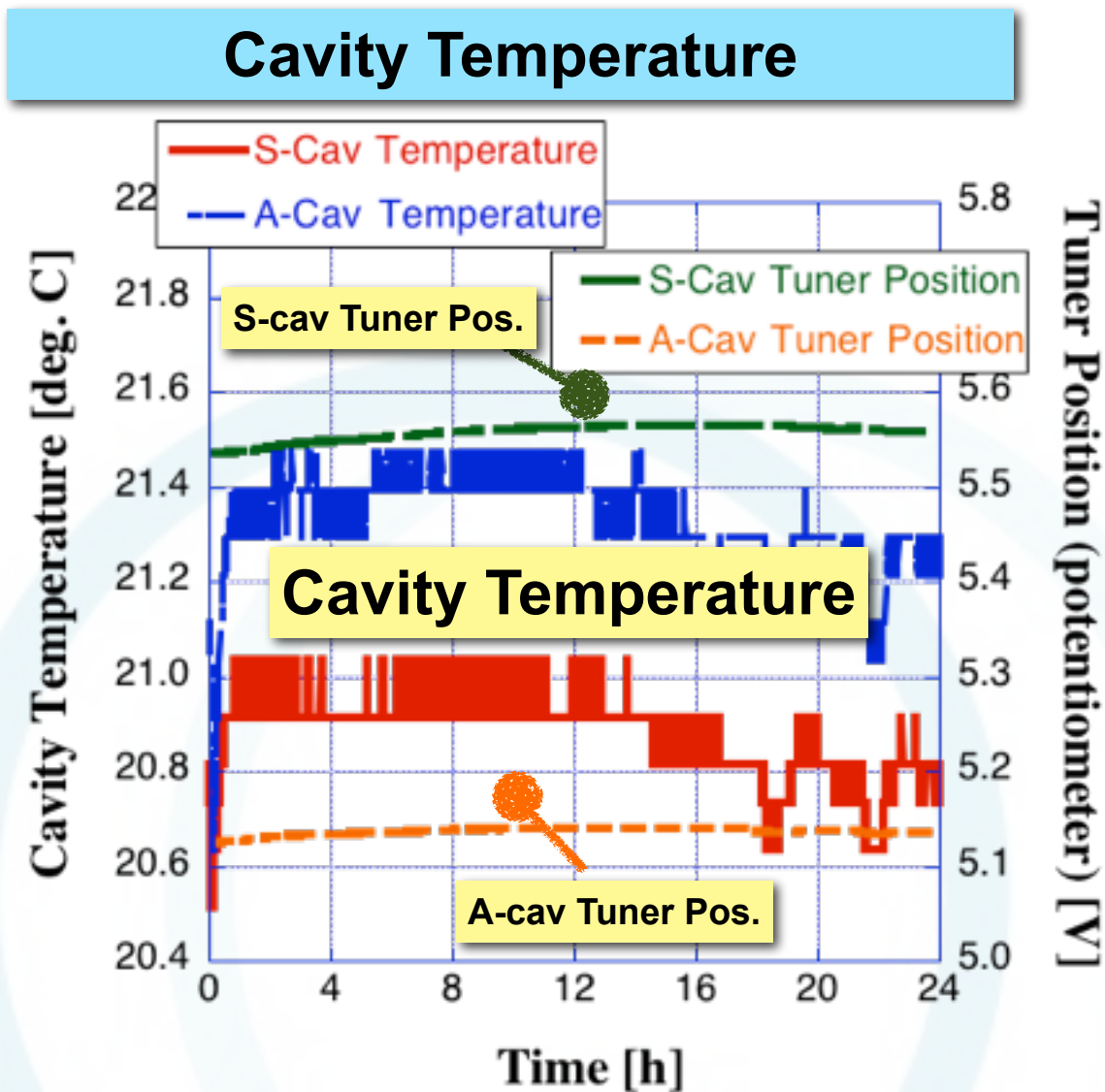
Improvement will be verified in next test model.

ARES 100W Drive Test for FB & Tuner Control



Running Test of ARES Auto Tuning by 100W Driving (not High Power)

Trend graph for 2 days



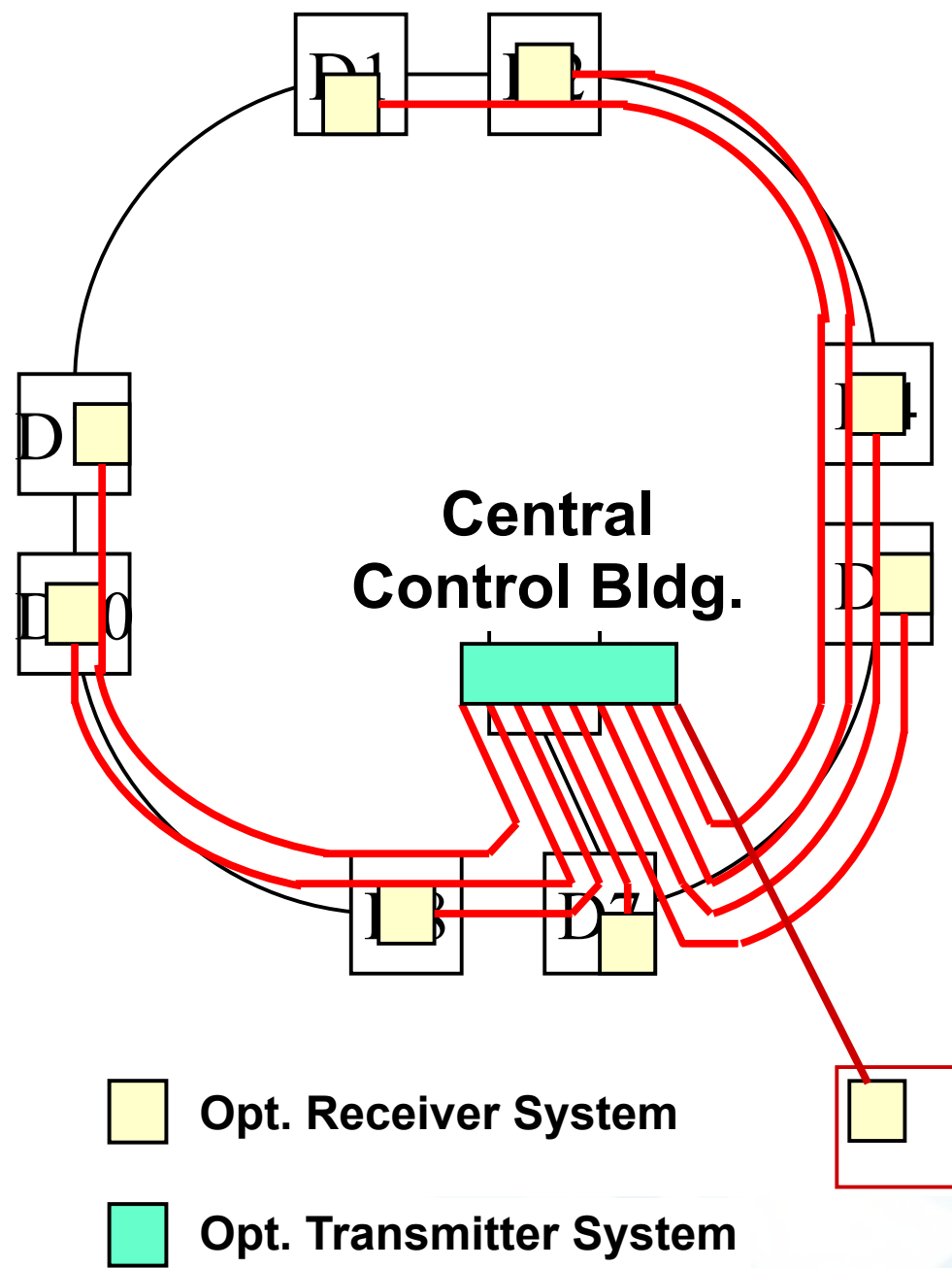
Cavity temperature change is small. (It is maybe due to ambient temperature.) Also tuner moved slightly to keep tuning. This tuner position change corresponds to about 15 degrees of the storage cavity.

Auto tuner controller of FPGA board worked successfully.

RF Reference Distribution

The details are under consideration now.

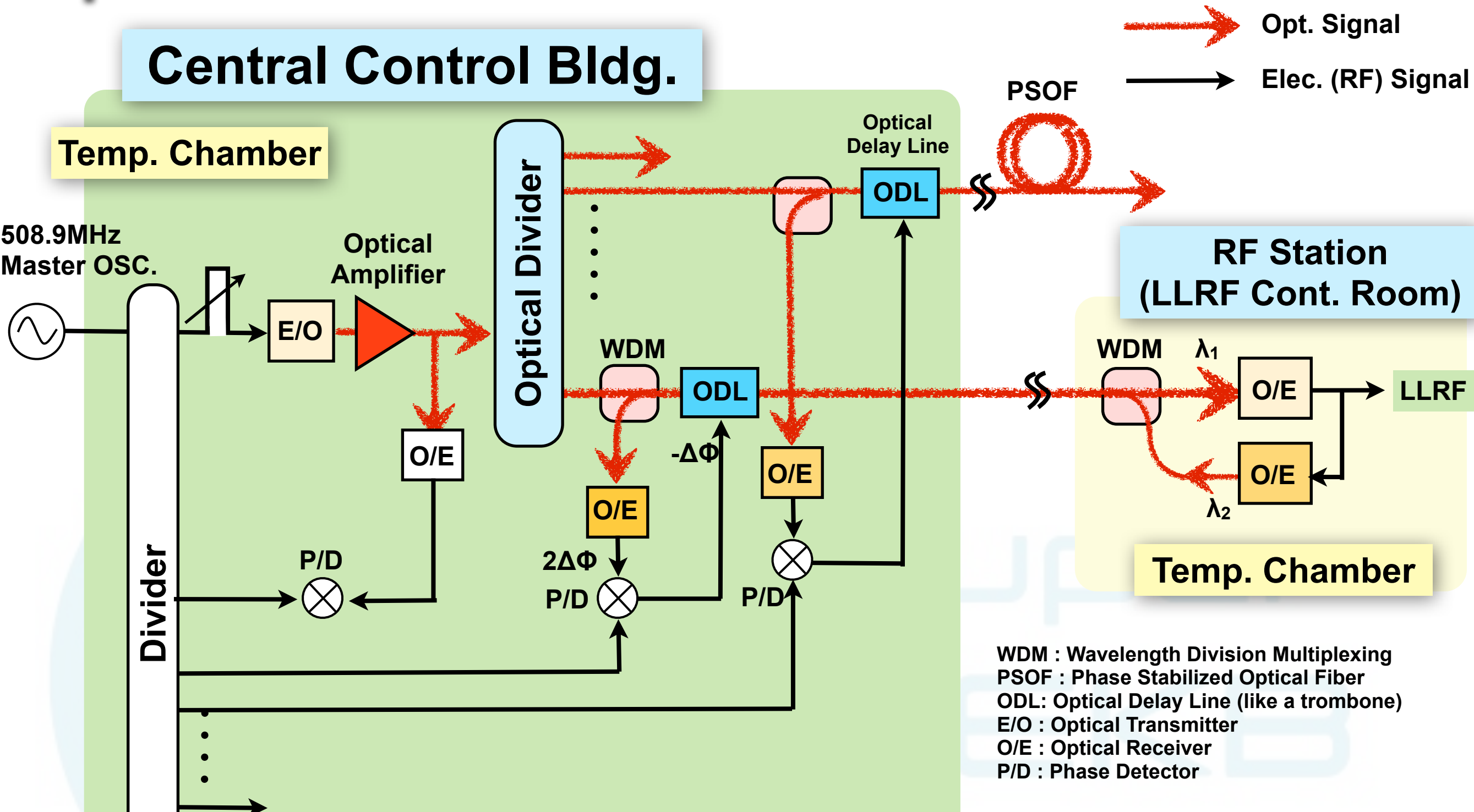
Design Concept



- Optical Distribution (Master OSC. -> E/O -> O/E)
- Phase Stabilized Optical Fiber (PSOF) will be used.
- The PSOF cables will be transferred in the acc. tunnel. (Temperature stability : +/- 1 deg.C)
- Distributed by means of "Star" configuration.
- Phase FB control will be implemented to compensate temperature drift of the cable if necessary.

Present reference system is maintained for the backup.

Optical Reference Transmitter & Receiver



As the phase detector, digital direct sampling method is proposed.
 Temperature of the transceiver system should be stabilized.

Validity of these method and components will be studied and the specification will be fixed next fiscal year.

Summary

- **Prototype of the digital LLRF system for the SuperKEKB was developed, and its performance was evaluated.**
- **Very good stability of is obtained in FB control. (0.03% in amp. & 0.02 deg. in phase)**
- **But, temperature dependency is not negligible. Some countermeasures should be studied.**
- **Auto Tuner Control given by the FPGA works successfully. (Piezo tuner control is not yet tested.)**
- **Optical RF reference distribution system is under consideration. The detail specification will be fixed next fiscal year.**

Next model for the quantity production (β version) is in the process of fabrication now.

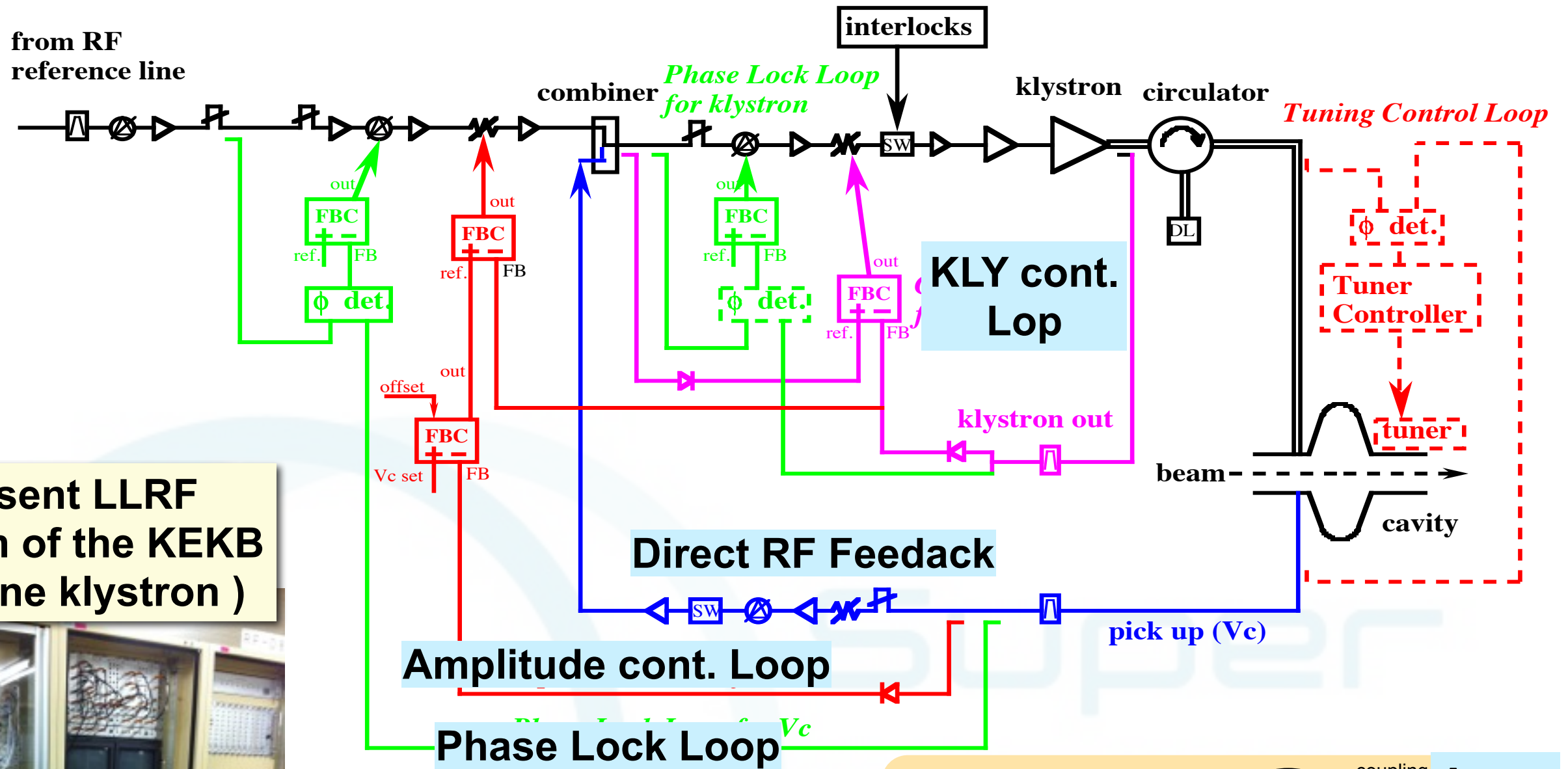
Thank you for your attention !



Followed by Backup Slides

Super
KEKB

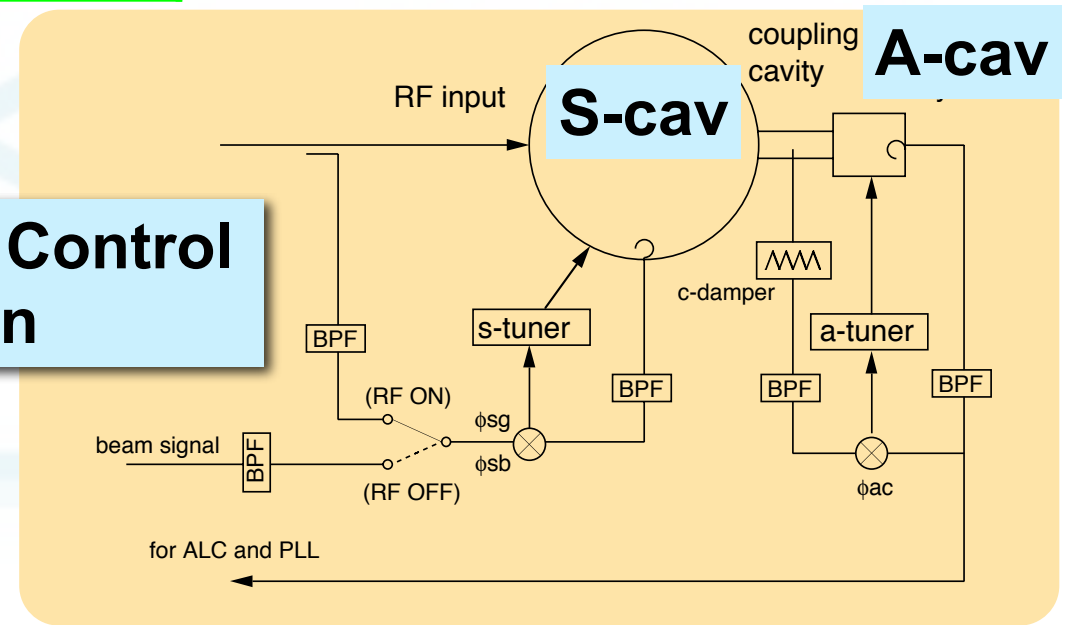
KEKB-LLRF System (Present)



Present LLRF System of the KEBB (for one klystron)

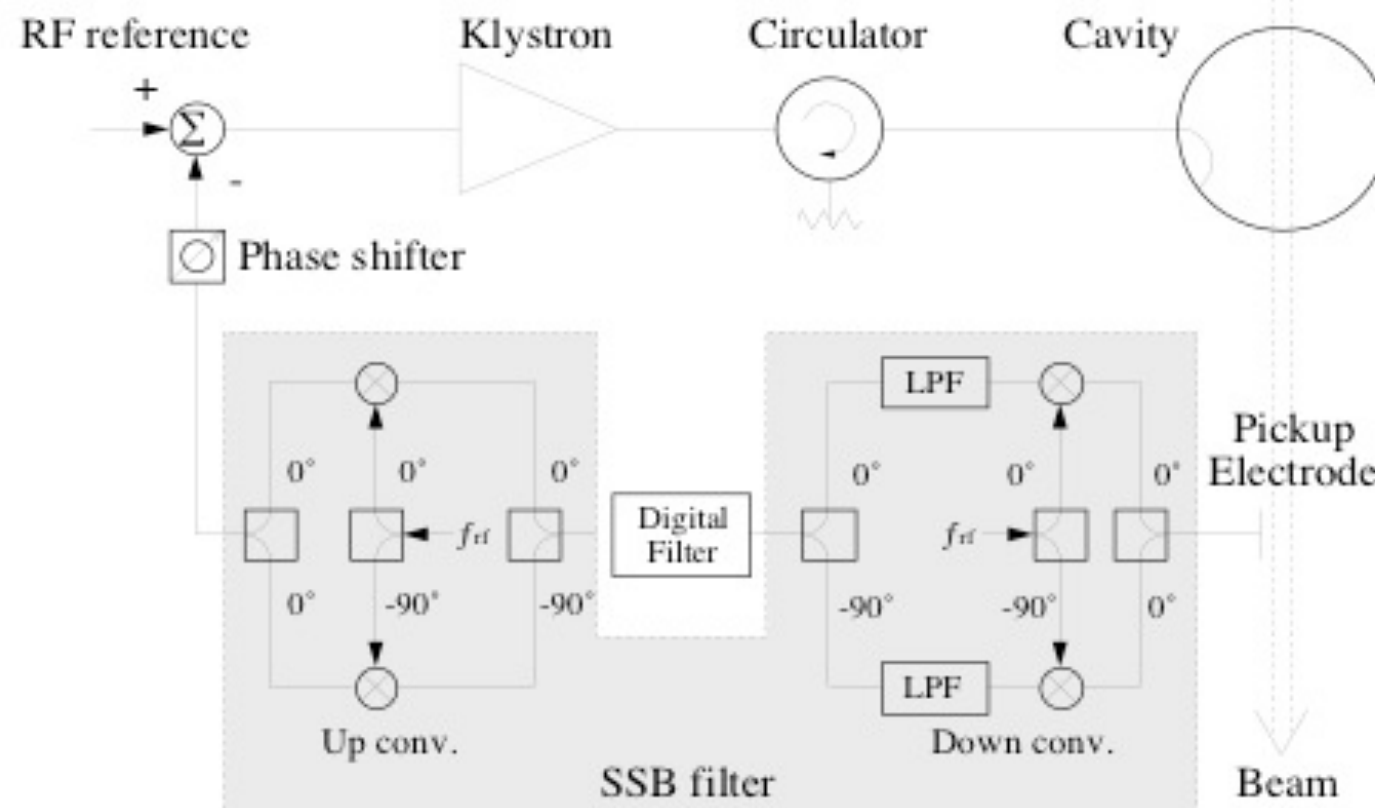
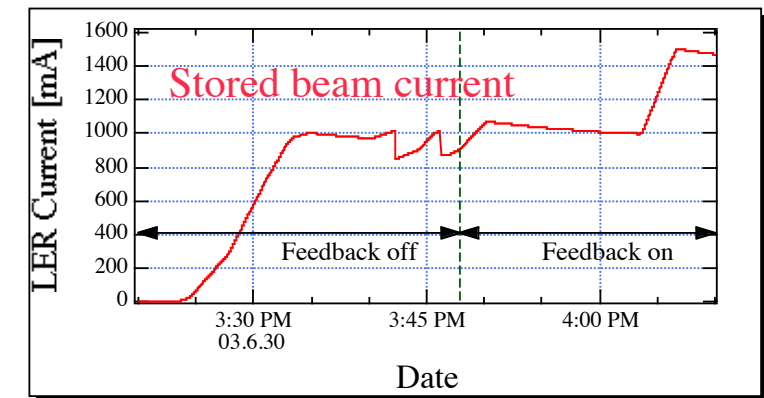


ARES Tuner Control Configuration

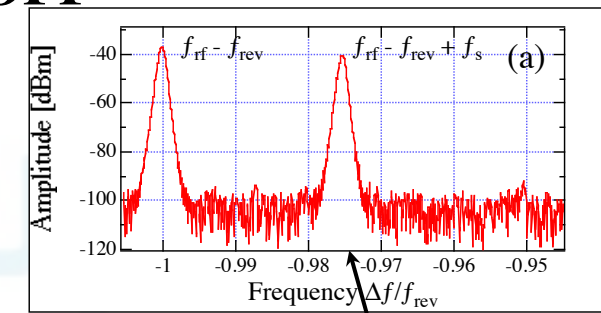


The -1 mode feedback

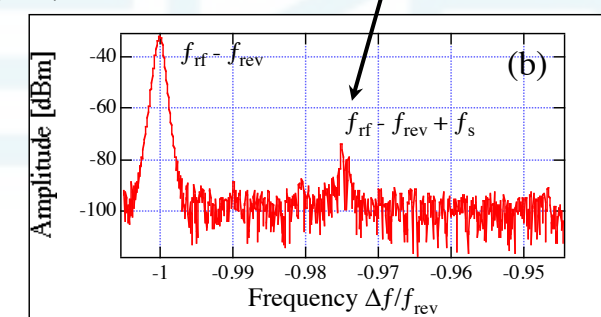
- Beam current was limited due to the -1 mode instability at 1 A in LER and 1.2 A in HER, much lower current than expected.
- The -1 mode digital feedback selectively reduces impedance at the driving frequency.
- After the -1 mode feedback was installed, the beam current could be successfully increased.



FB OFF

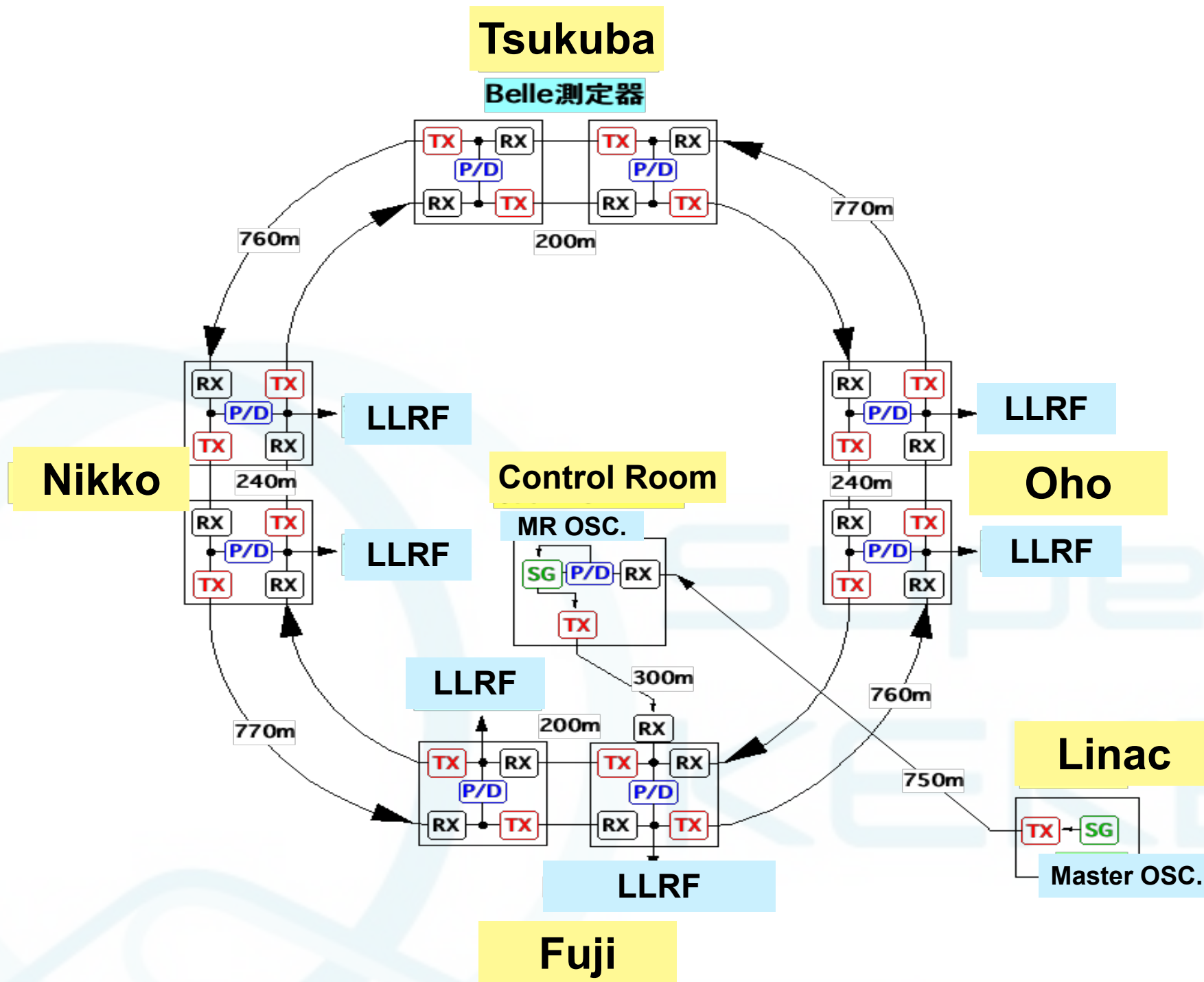


FB ON



-1 mode sideband

KEB RF Reference System



- TX Transmitter
- RX Receiver
- P/D Phase Detector

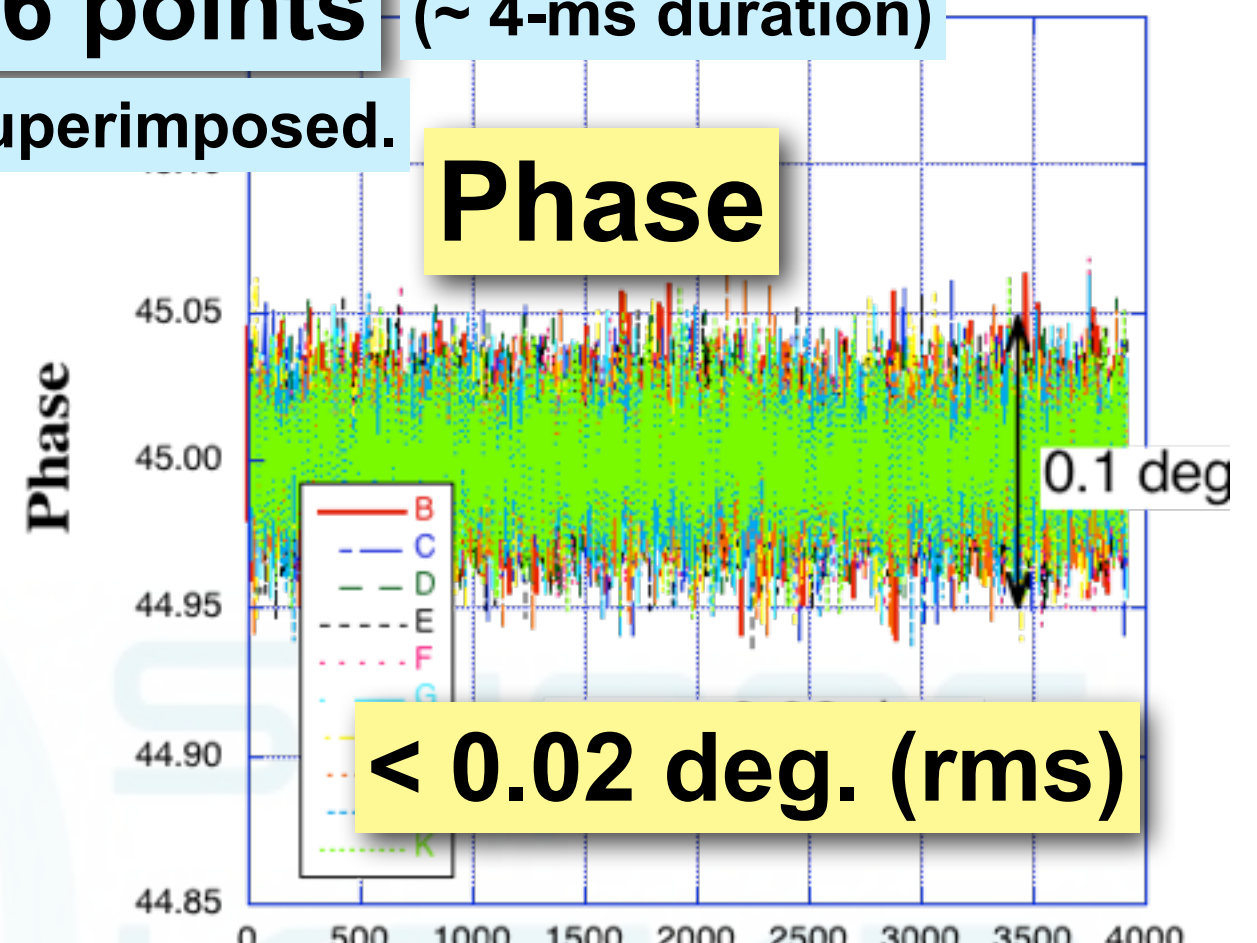
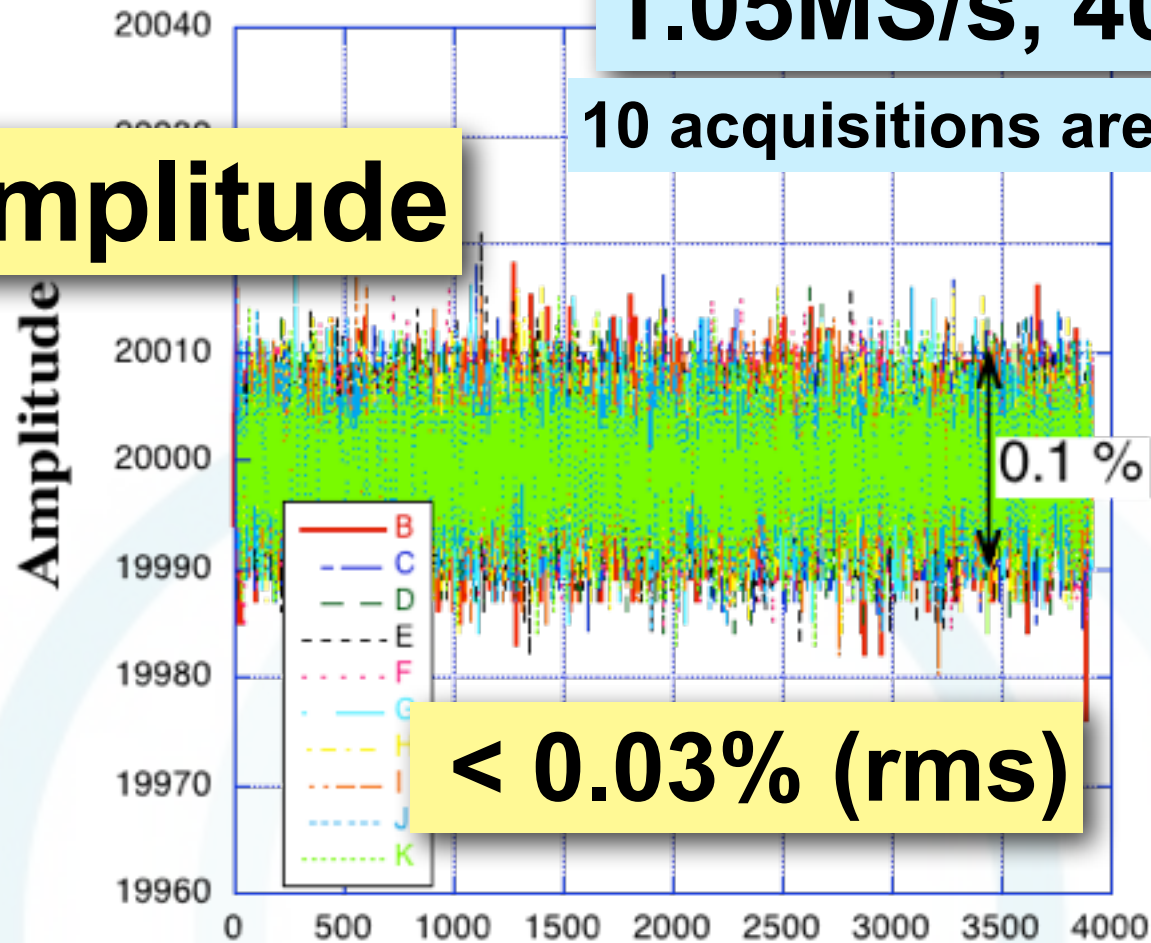
DFT of the waveform

1.05MS/s, 4096 points (~ 4-ms duration)

10 acquisitions are superimposed.

Amplitude

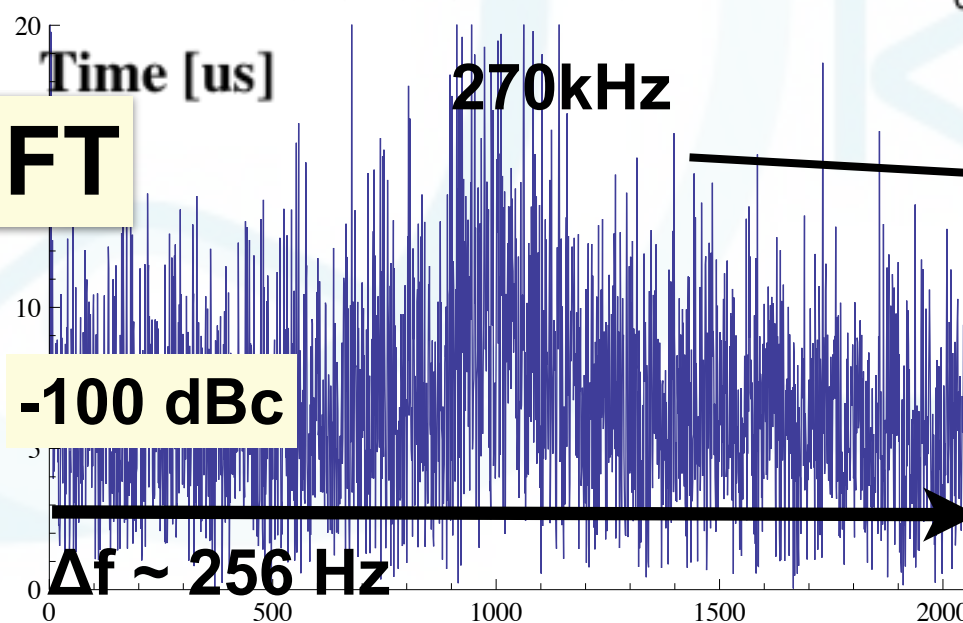
Phase



FFT

-100 dBc

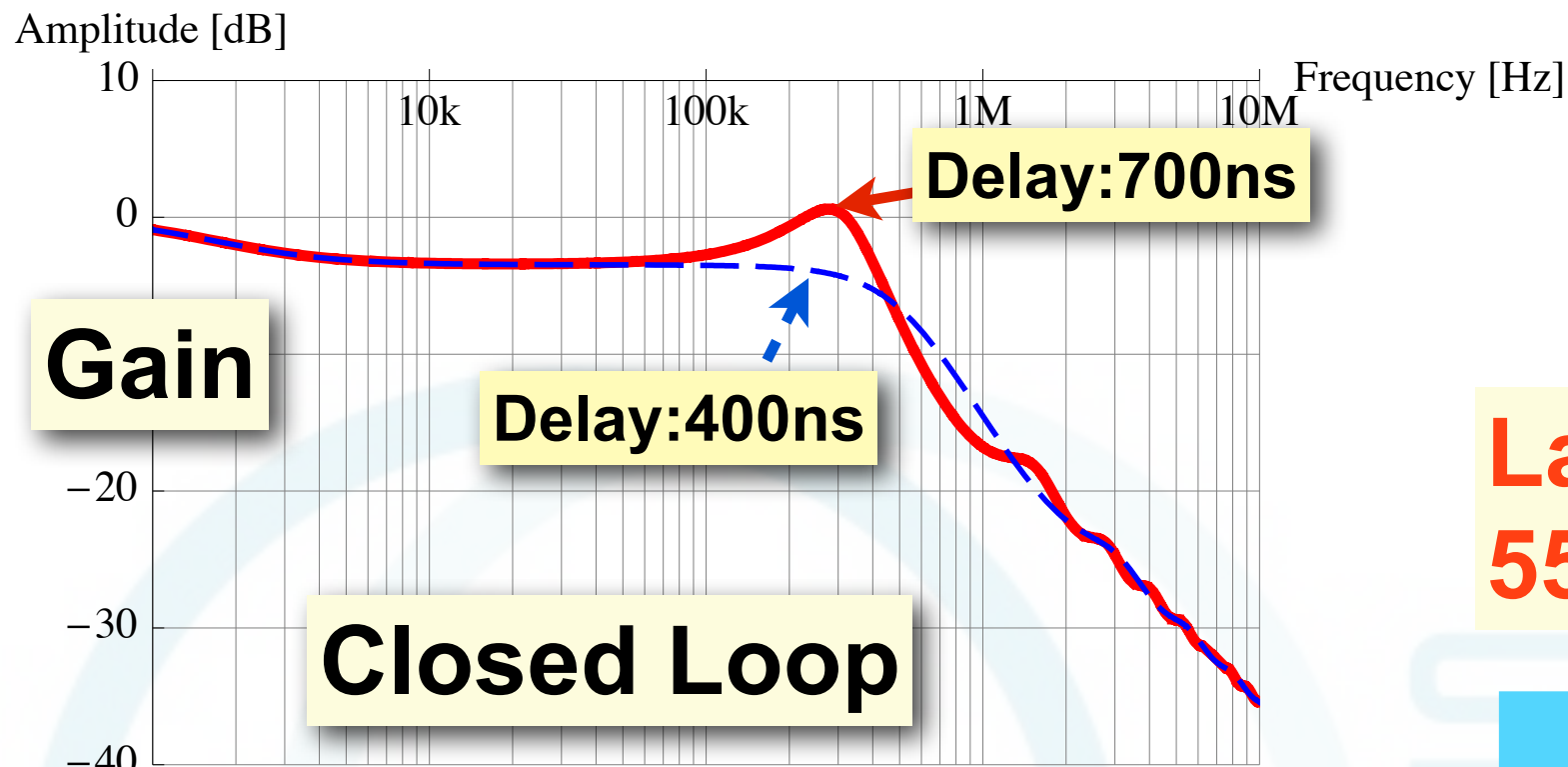
$\Delta f \sim 256$ Hz



Due to the latency of the FPGA and DAC, which makes 650ns-loop delay. No problem for the ARES Cavity ($Q_L \sim 20000$).

Bode Plot for the Simulant Cavity ($Q_L \sim 3000$)

$$P_{\text{gain}}=2, I_{\text{gain}}=2.6 \times 10^4$$



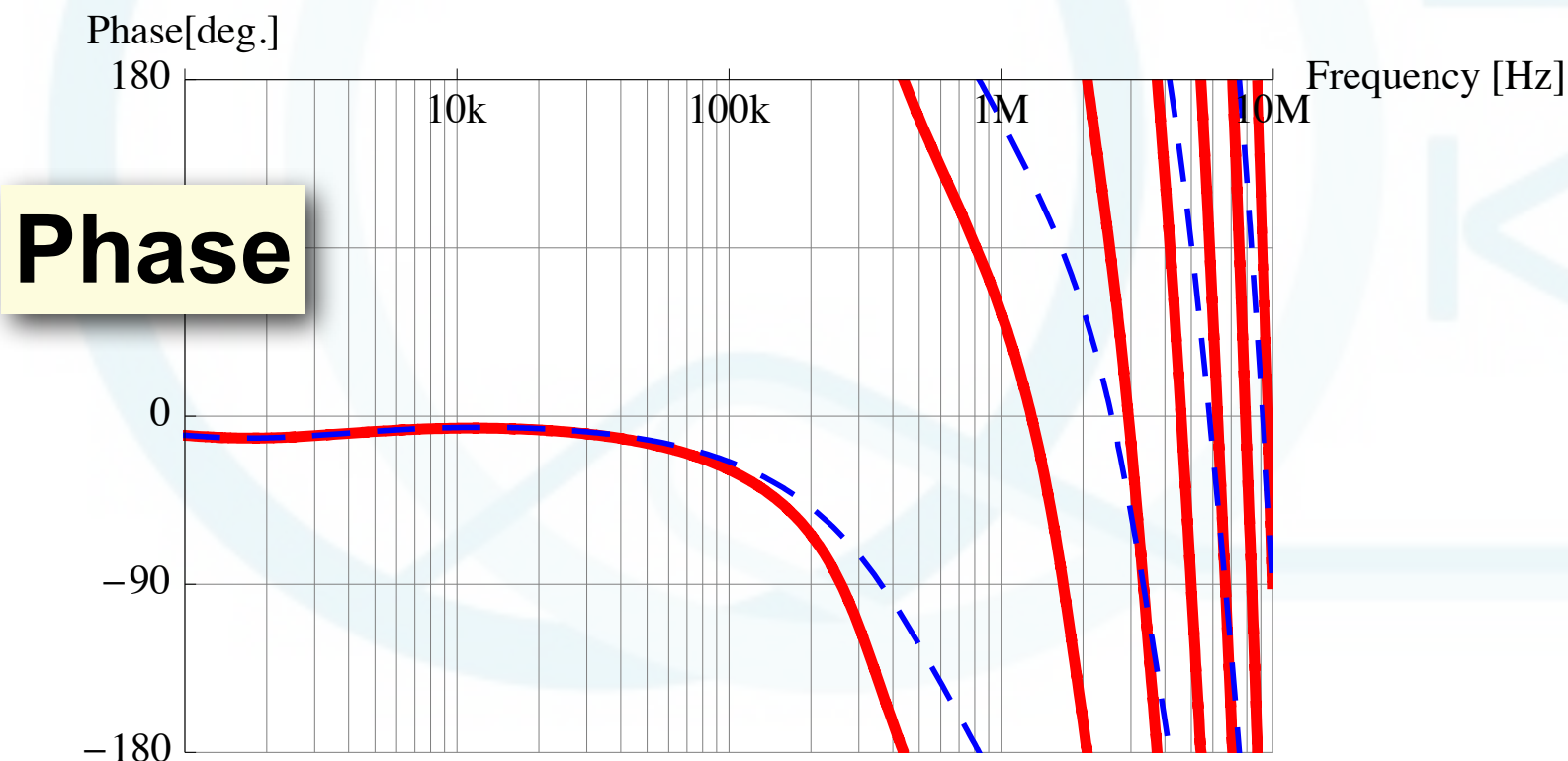
$Q_L=3000$

$\Delta\omega = 0$

Loop Delay = 700ns

Latency in the FPGA :
55 clock

Loop Delay :
~650ns

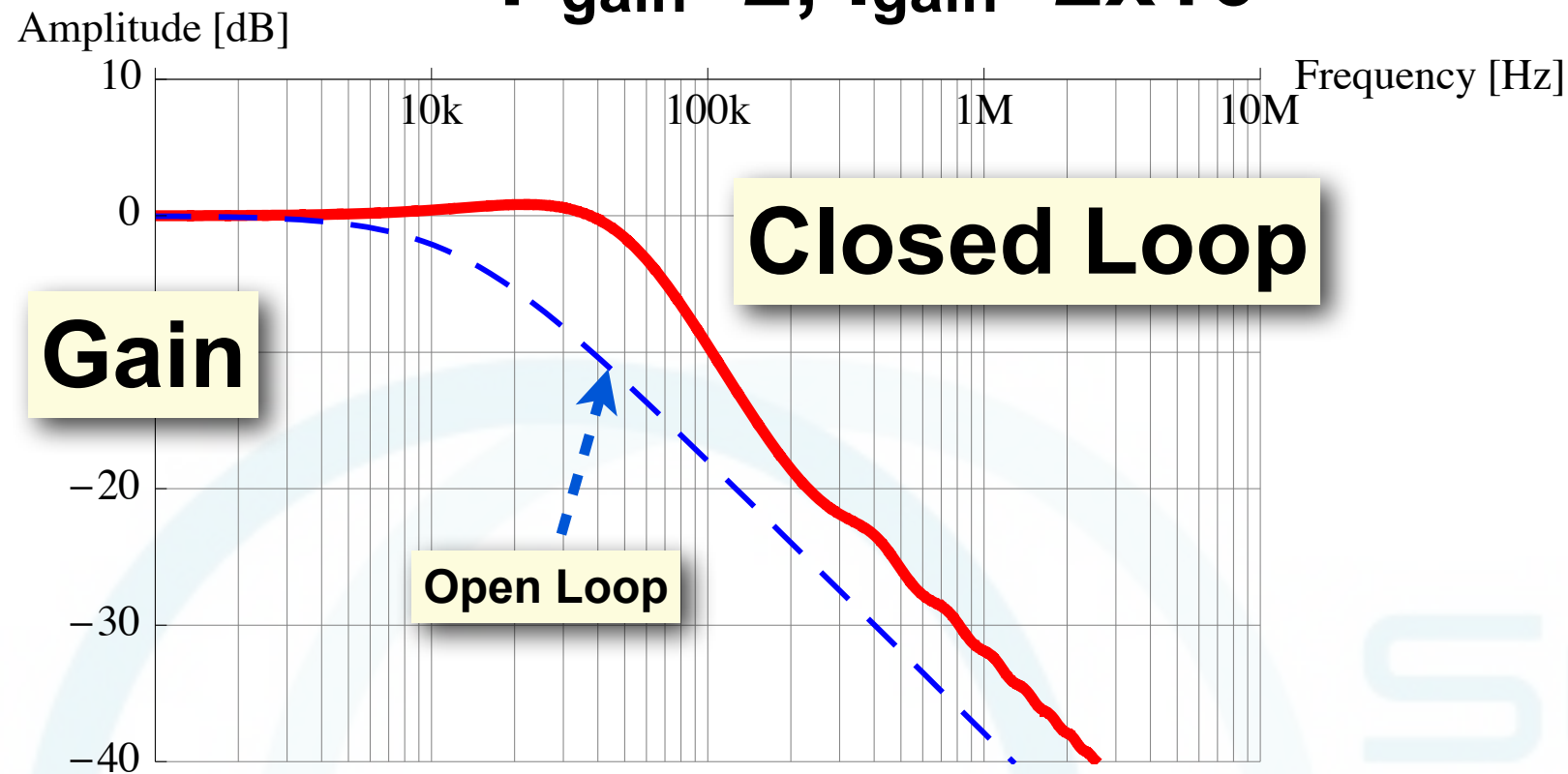


Gain Margin :
~13dB

$P_{\text{max}} \sim 2.2$

Bode Plot for the ARES ($Q_L \sim 20000$)

$$P_{\text{gain}}=2, I_{\text{gain}}=2 \times 10^5$$



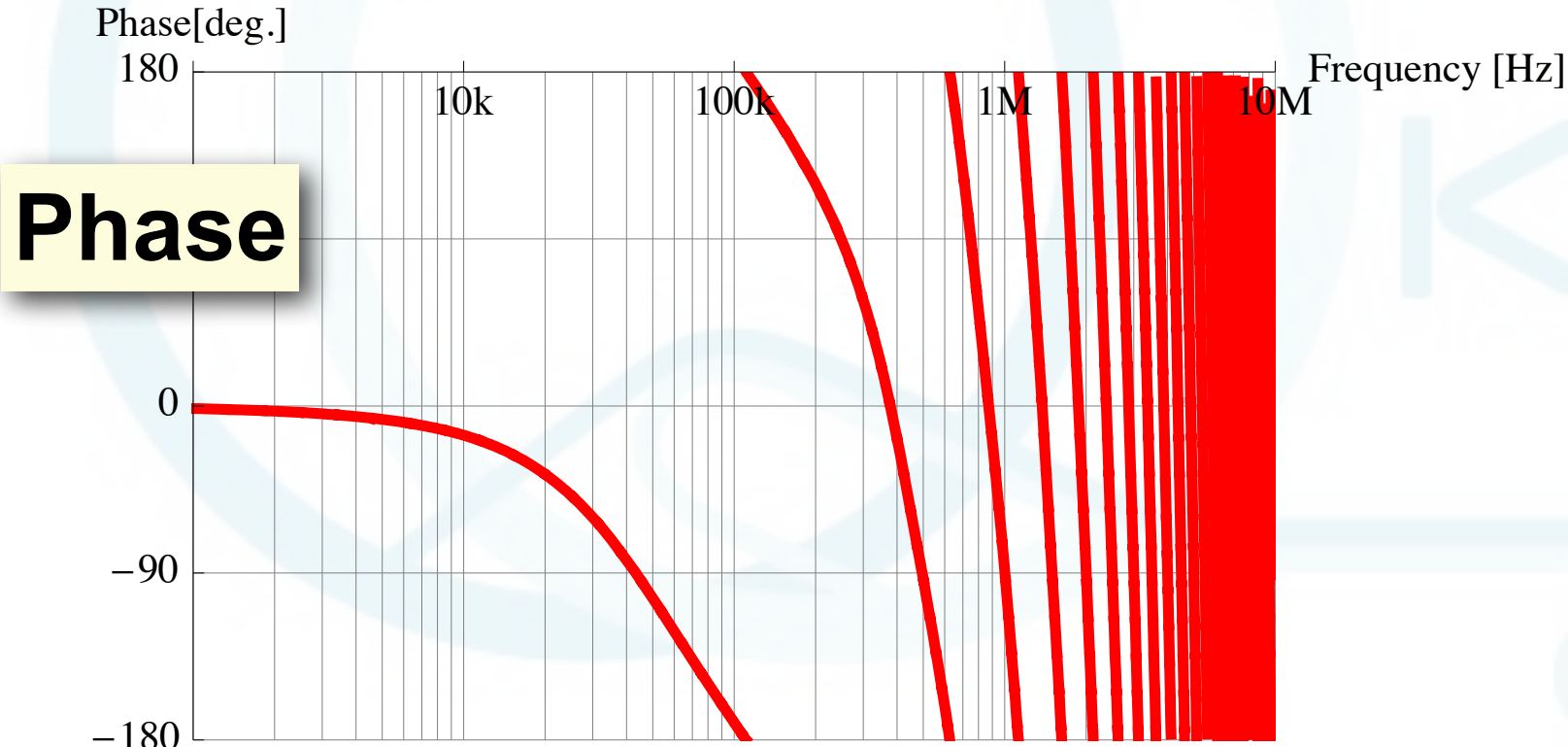
$$Q_L = 20000 \quad \Delta\omega = 0$$

$$(Q_0 = 120000, \text{Coupling} = 5)$$

$$\text{Loop Delay} = 3\mu\text{s}$$

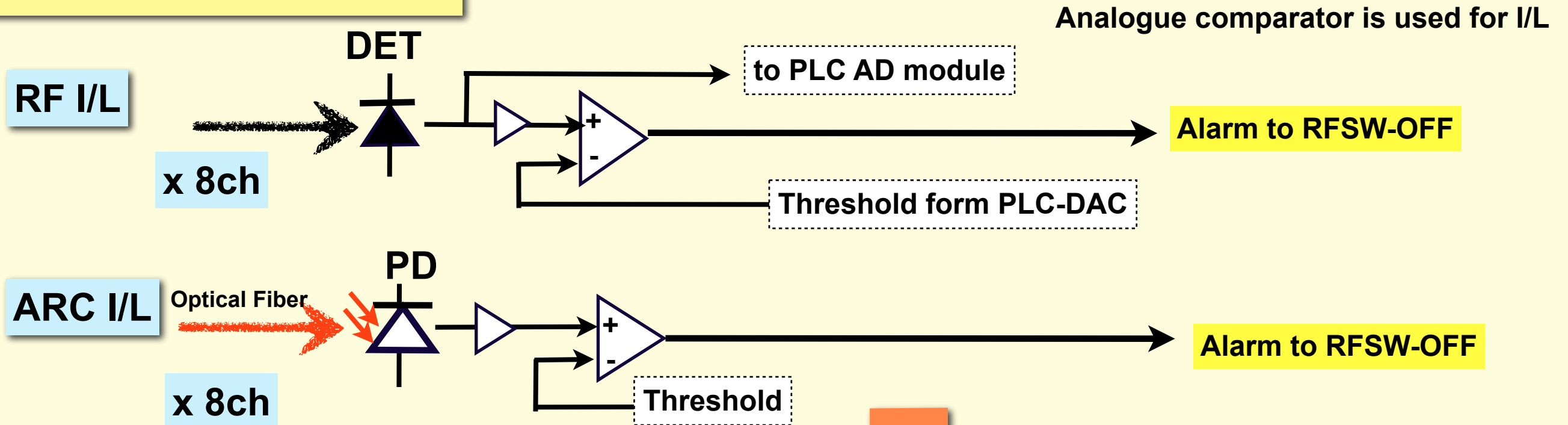
$$\text{Gain Margin : } \sim 18\text{dB}$$

$$P_{\text{max}} \sim 4$$



RF & ARC Inter Lock

α version



β version

