The 19th KEKB Accelerator Review Committee (2014.03.04)

Status of LLRF System

~ KEKB LLRF Team ~

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Outline

1. Overview & Status
2. Klystron Phase Lock Loop (KLY-PLL)
3. Response (Frequency) Property of FB control
4. Bunch Gap Transient Effect
5. Schedule & Summary

Given comments in the report of last KEKB ARC

1. What happens if the LLRF system doesn't boot up orload the FPGA properly, or some software process hangs up? (Interlocks should be very robust and not a software function).

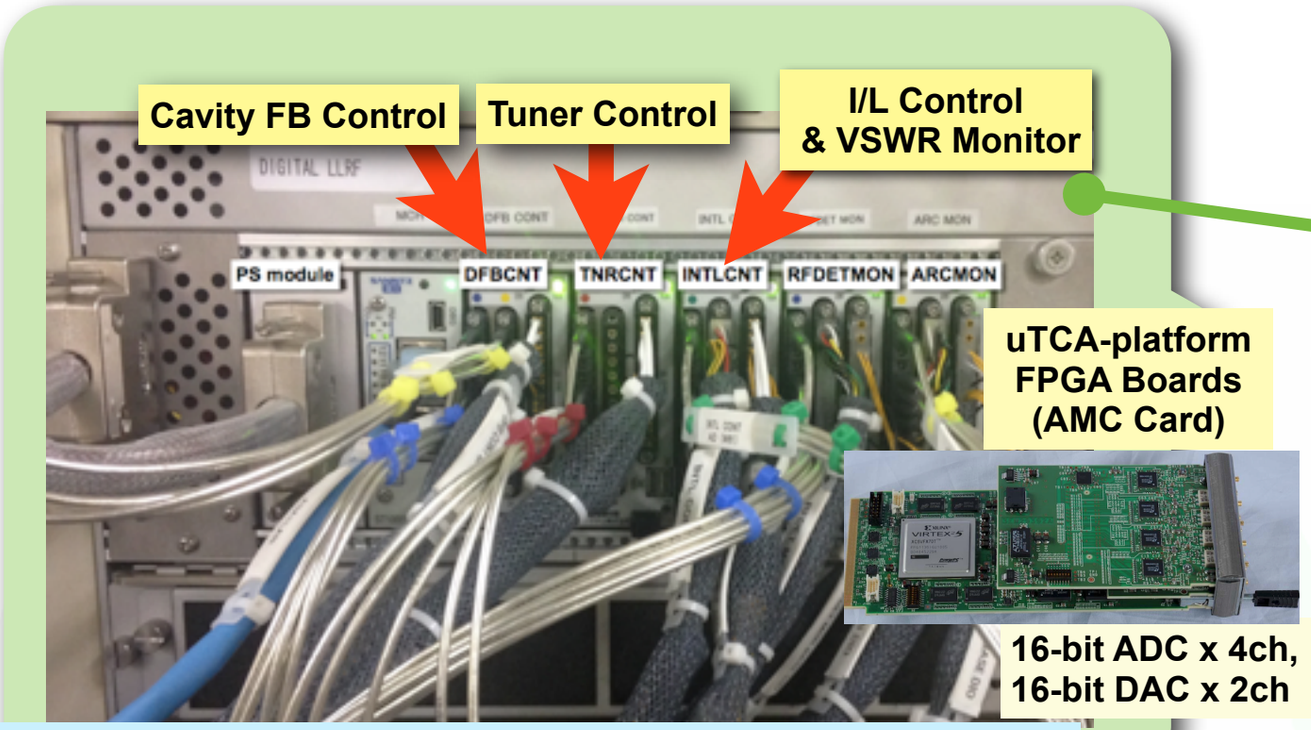
2. Dynamic responses of the closed loop system? (information in the frequency domain?)

3. Bunch gap transient effects? Is the shift of the IP (the difference between the HER and LER) acceptably small?

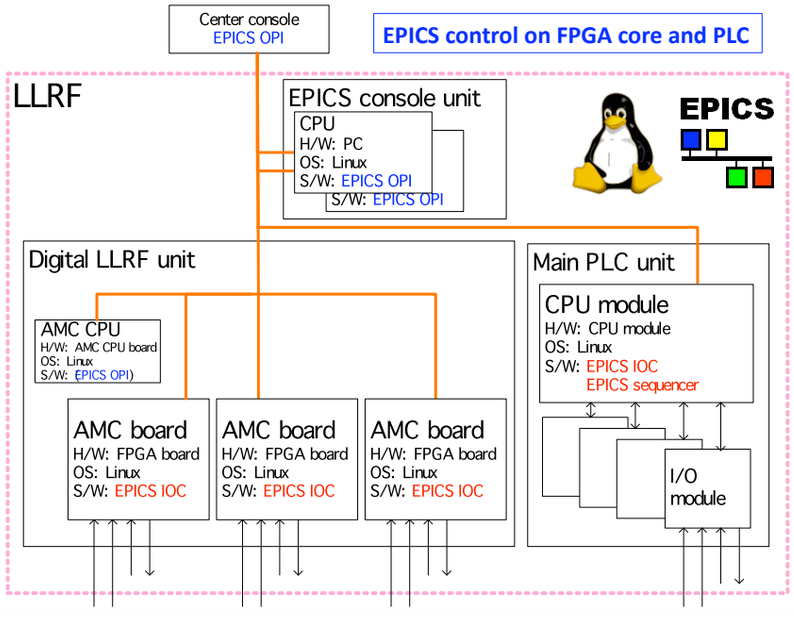
New LLRF System for SuperKEKB

Preset analog systems will be replaced by new digital ones step-by-step.

A new LLRF system has been developed and the performance was evaluated.

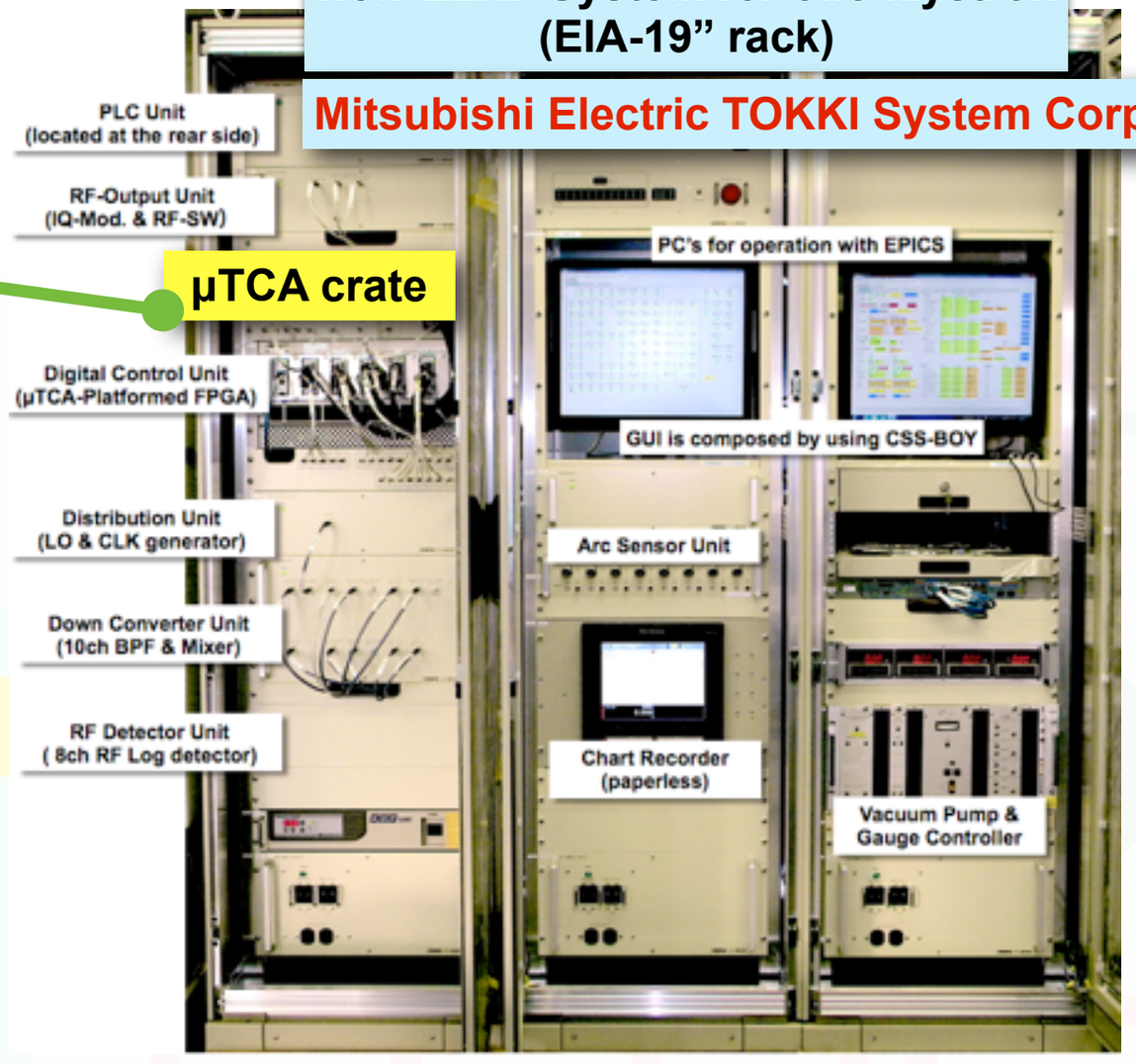


Each board has a CPU (PPC), and the EPICS-IOC on Linux-OS is embedded.



New LLRF System for one klystron (EIA-19" rack)

Mitsubishi Electric TOKKI System Corp.



- **This system consists of μTCA-based FPGA boards & PLC.**
- **EPICS-IOC on Linux-OS is embedded in each of them. They can be operated remotely via EPICS-Channel Access.**
- **Hardware is common for both of ARES & SC Cavity. (Also both softwares are much the same.)**
- **Klystrons (LLRF) : Cavity unit = 1 : 1 (SuperKEKB)**

Block Diagram of FB&Tuner Control for ARES

LLRF System

PTG : Pulse Train Generator

cw/ccw

10V 1kHz

cw/ccw

Tuner Driver

RF Reference

508.9 MHz

RF : 508.9 MHz

-1 Mode FB

508.8MHz

I/Q Mod.

Combiner

FPGA (Kly P_f, VSWR, Ard, ...)

PLC (Water, Vac., Temp., ..)

Inter Lock

RF-SW

Driver Amp

KLY

Arc sensor

Arc sens.

Tuner

ARES Cavity

A-Cav

Arc sens.

S-Cav

C-Dmpr

Tuner

LLRF P_{for}

D-Amp P_f, P_r

Kly P_f, P_r

Cav P_{cav}, P_r

uTCA-based FPGA boards

I

Q

Tuner Cont.

PTG (S)

PTG (A)

DAC

DAC

FB Cont.

Rotation

FF- I

FF- Q

P-gain

P-gain

ΔΦ (s-g)

ΔΦ (a-c)

tune offset

PI - Cont.

DCCT

Ref-I

Ref-Q

Rot.

I,Q

ADC

Selector

ADC CLK 4 x IF

IF

I

-Q

Q

-I

I,Q Detection

CLK

1/6

CLK

84.8 MHz

LO & CLK Distributor

1/2

CLK

42.4 MHz

1/4

LO

IF 10.6 MHz

LO : 519.5 MHz

LO

KLYout FWD

LO

A-Cav PickUp (a)

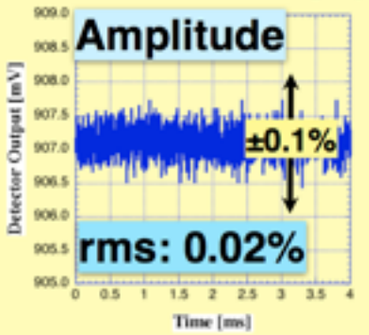
C-Cav PickUp (c)

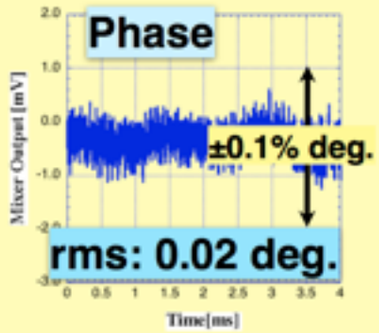
S-Cav PickUp (s)

Cav-Input (g)

Reported '13

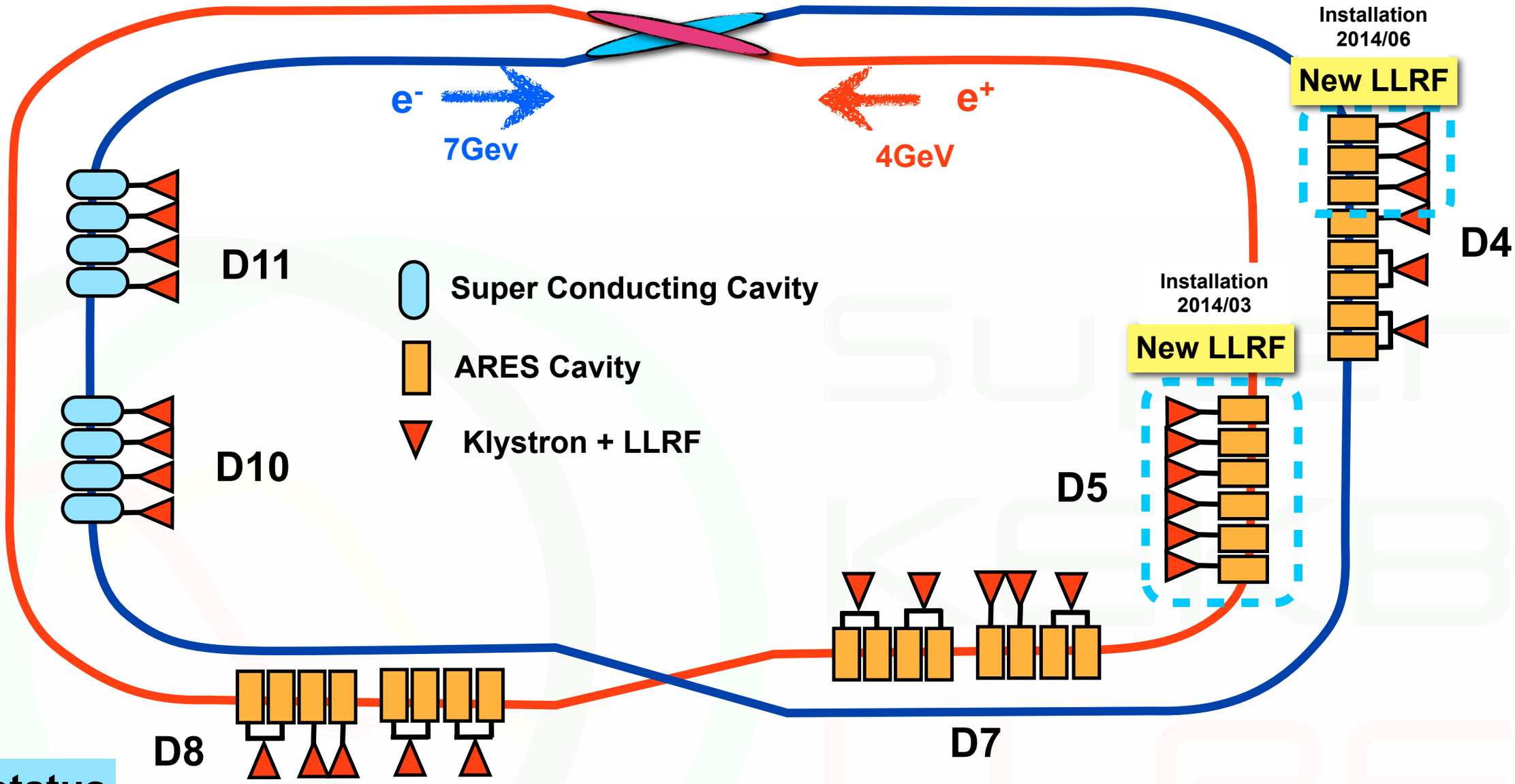
ARES Cavity FB Control Stability measured by external "outside-the-loop" monitor in high power test.





RF System Arrangement for Phase-I

In the beginning, New LLRF systems will be applied to 9 stations at D4&D5



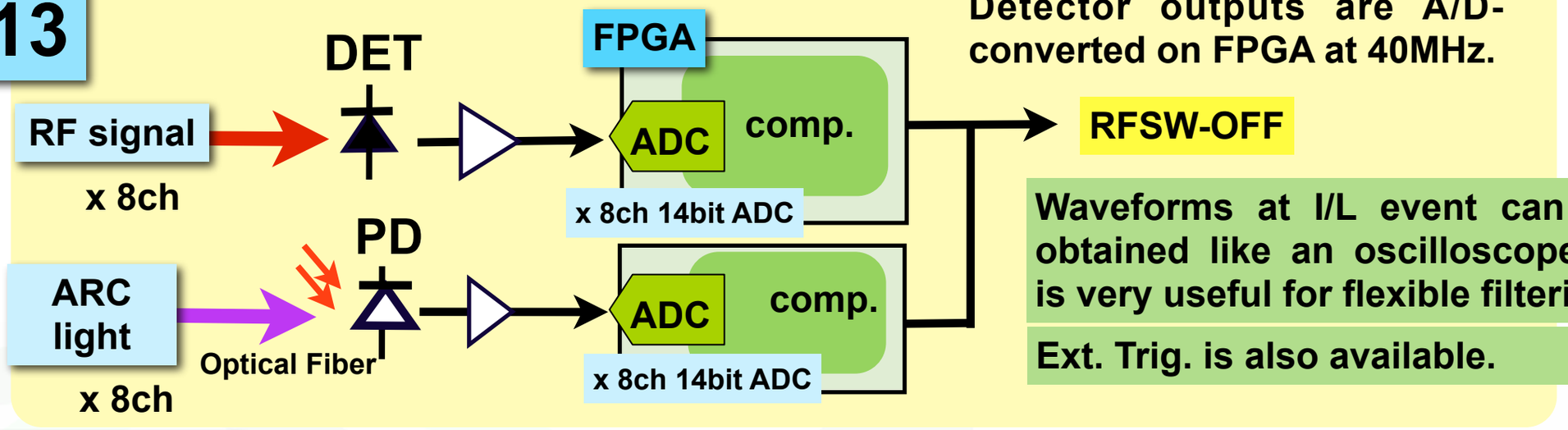
Present status

- Now the mass production of 8 systems is in progress as scheduled. And the prototype model (β-version) is also used for the operation at D4. They will be installed in March at D5 and in June at D4.
- The other stations are still driven by existing analogue systems.

- The DR-LLRF system will be produced next JFY. It is almost the same as MR one, except 3-cavity vector-sum control is needed.

Reliability of FPGA for Inter Lock

Reported ’13



Given comment

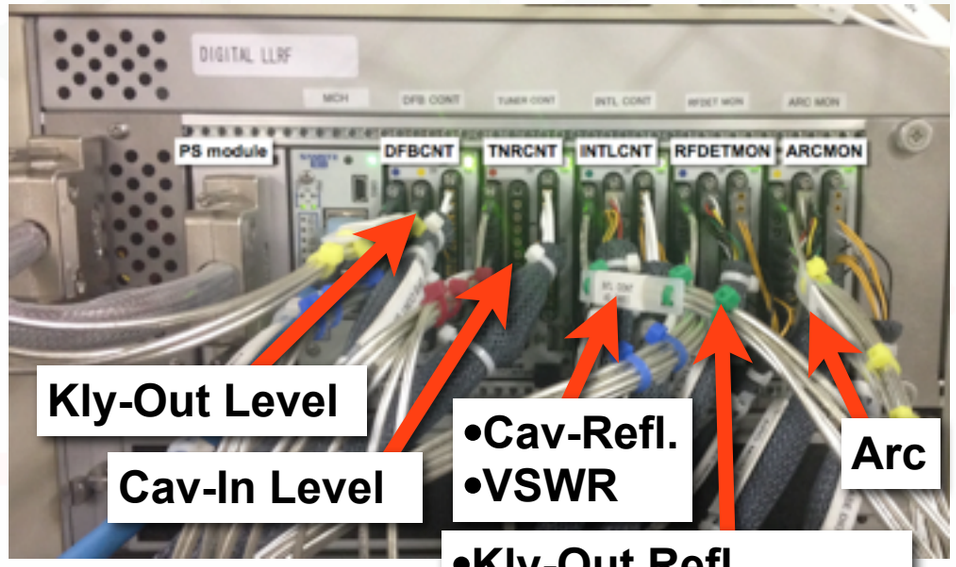
What happens if the LLRF system doesn’t boot up or load the FPGA properly, or some software process hangs up? (Interlocks should be very robust and not a software function).

Our viewpoint

FPGA is generally regarded as the same as hardware system, so it is very reliable.
It has accomplished solid performance in many fields.

It is hard to expect simultaneous hang-up of all FPGAs.

All boards have some I/L function (multiplexed). Any FPGA (or PLC) might detect some abnormal.

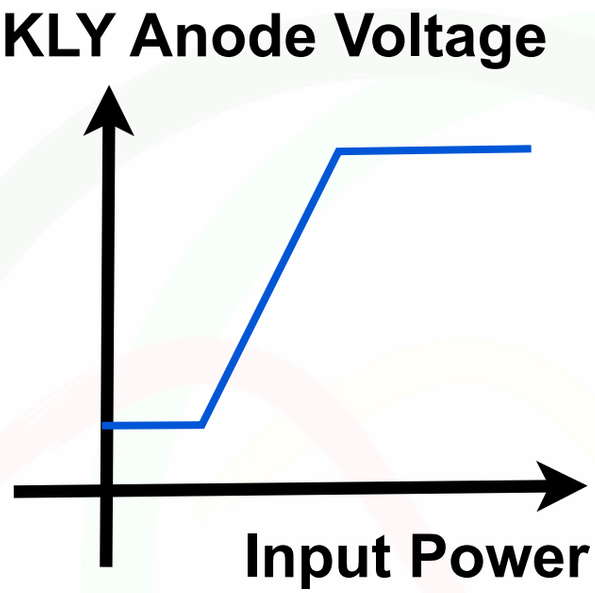


+ PLC I/L (Vac. water, etc..)

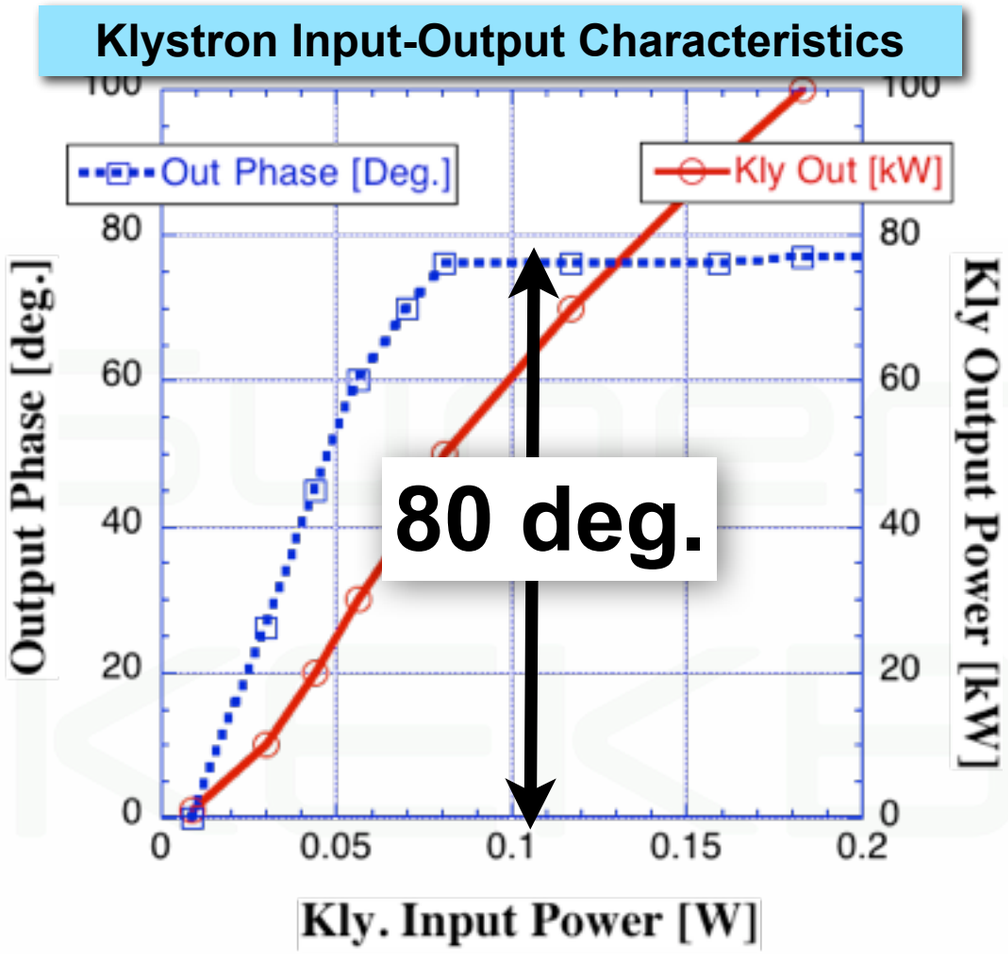
Reported ’13

Klystron Phase Change due to Anode Voltage Control

For efficiency optimization, the anode voltage is controlled depending on klystron input power to reduce the collector loss.



The kly. output phase shifts largely in response to input/ output power.



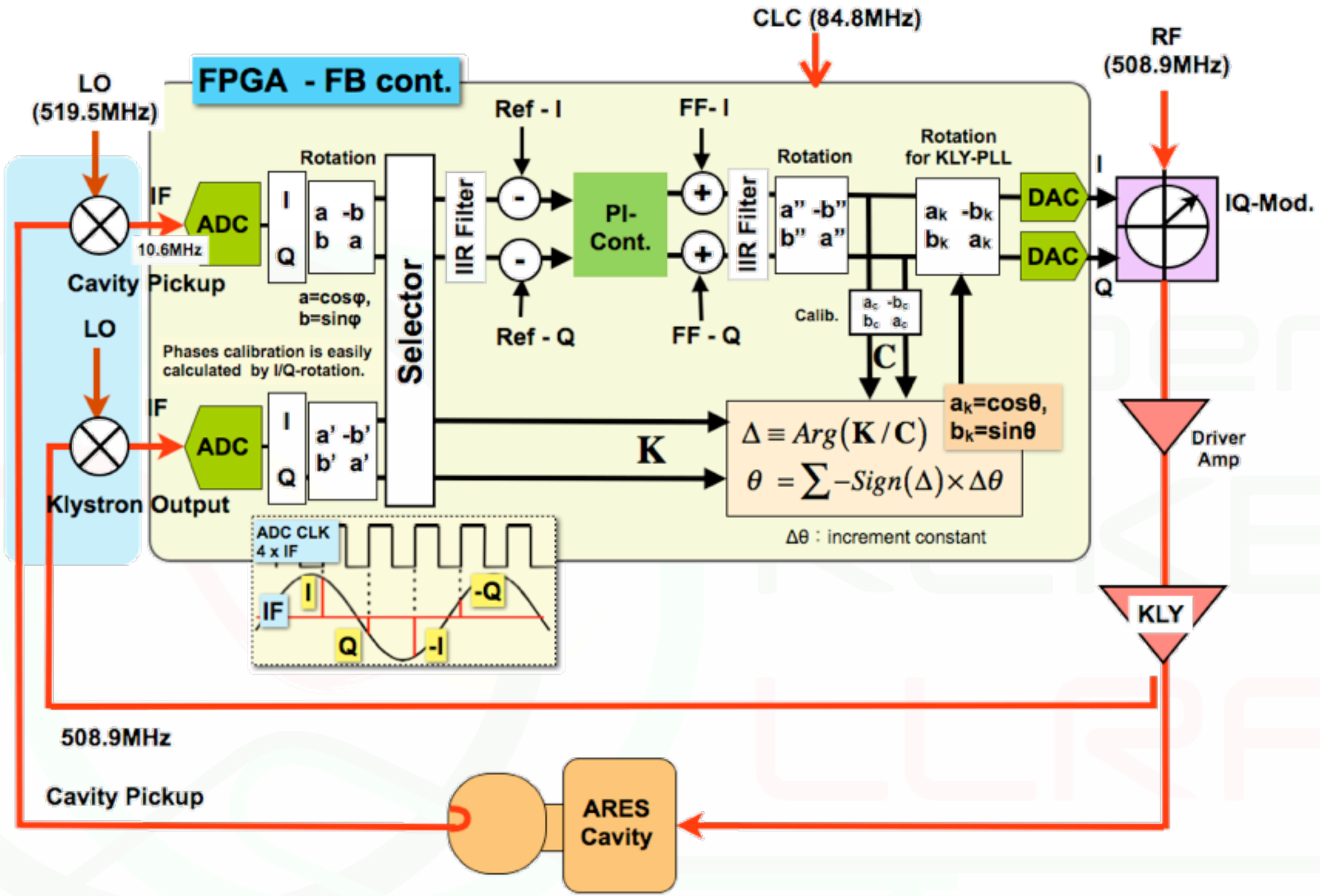
This phase change is unexpectedly-large.

The loop phase shift of 80 deg. will be critical problem for I/Q FB control technique.

(Acceptable phase change is about +/-60 deg.)

Klystron Phase Lock Loop (KLY-PLL) is necessary.

Implementation of Klystron PLL in FPGA

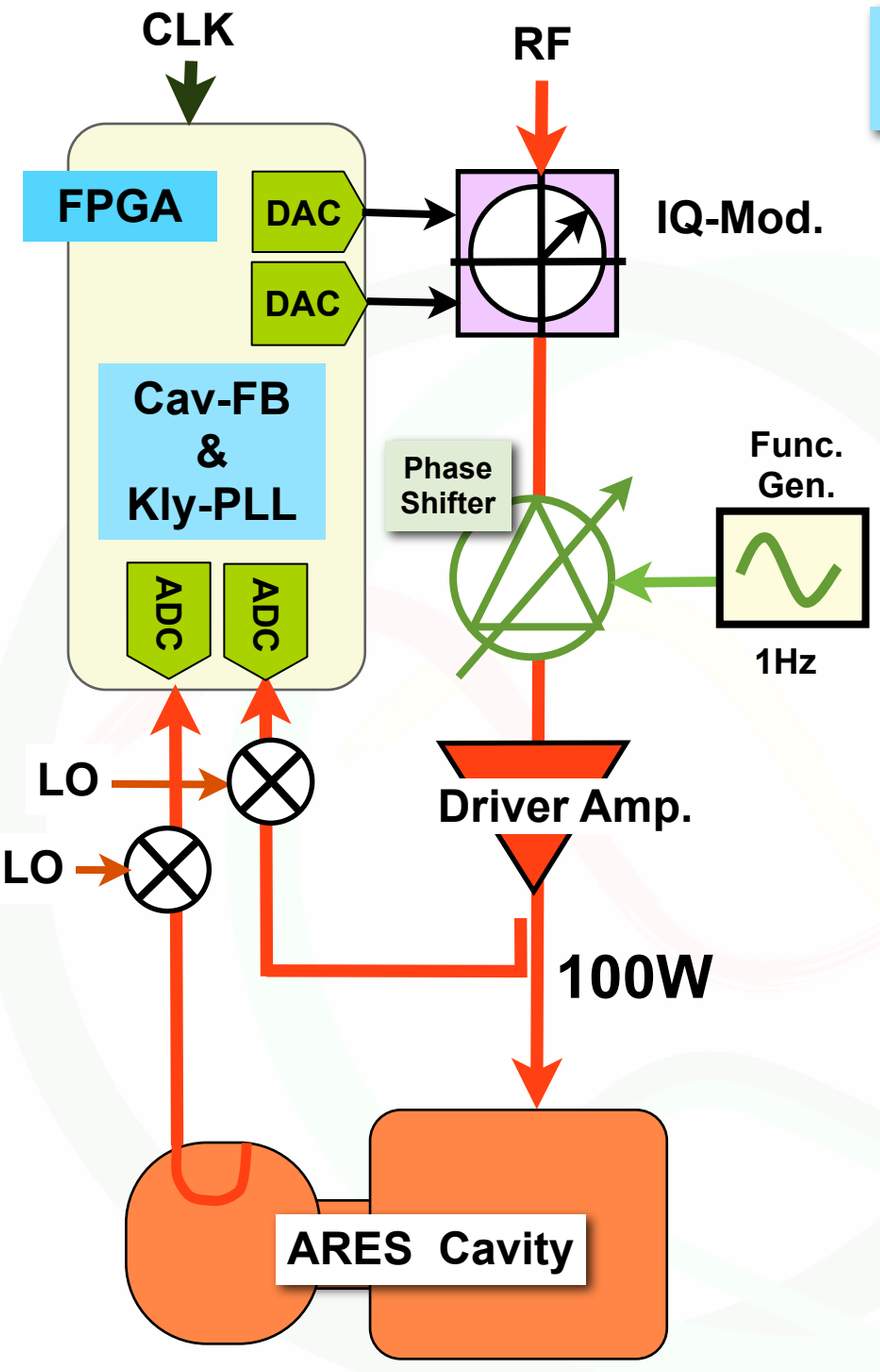


Required loop bandwidth : <1kHz (The anode voltage response : about 1Hz.)

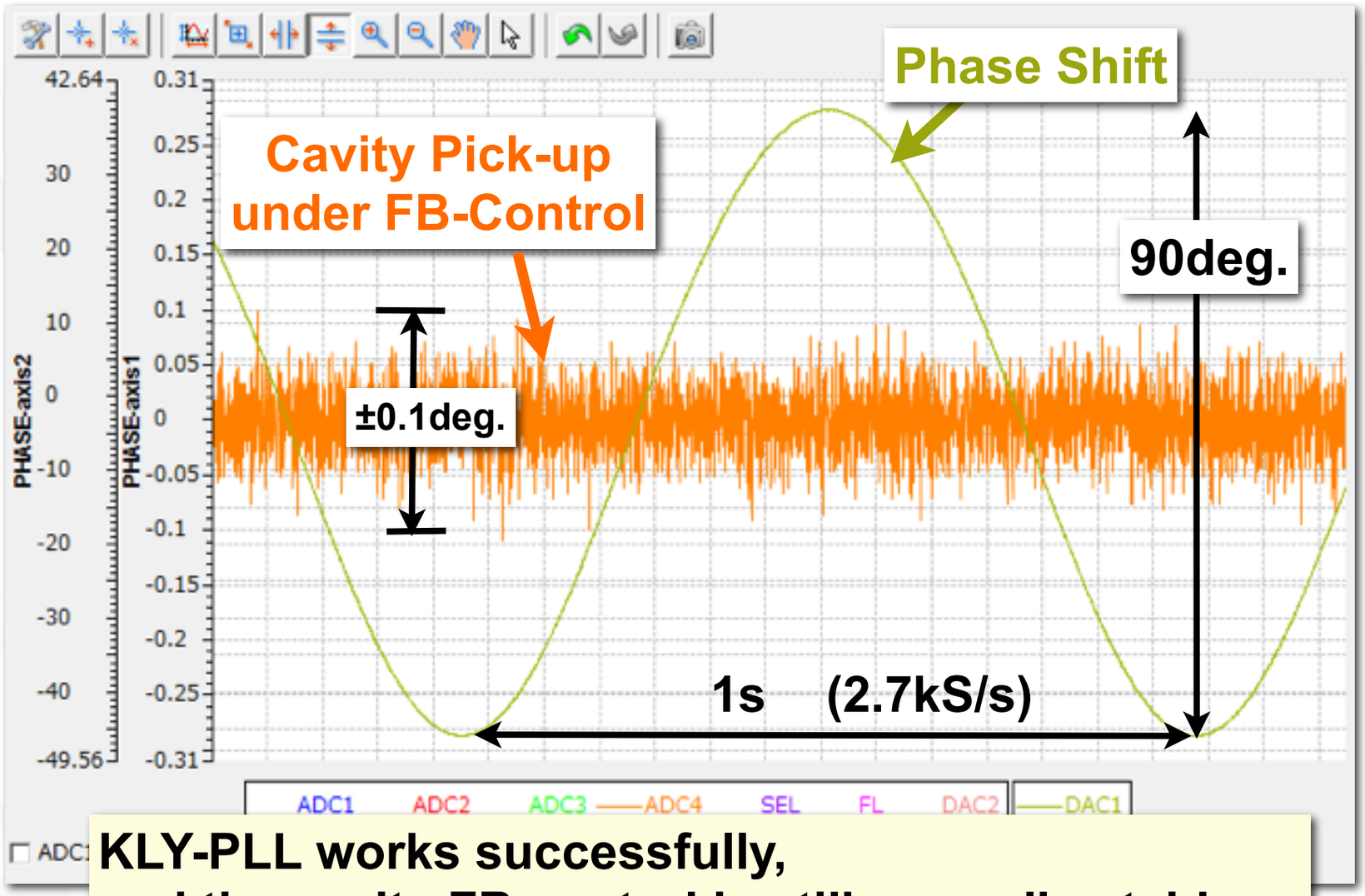
KLY-PLL Test Result with ARES-FB Control

in 100-W Driving

Cavity-FB & KLY-PLL acting together



Phase shift in the loop：90deg.@1Hz



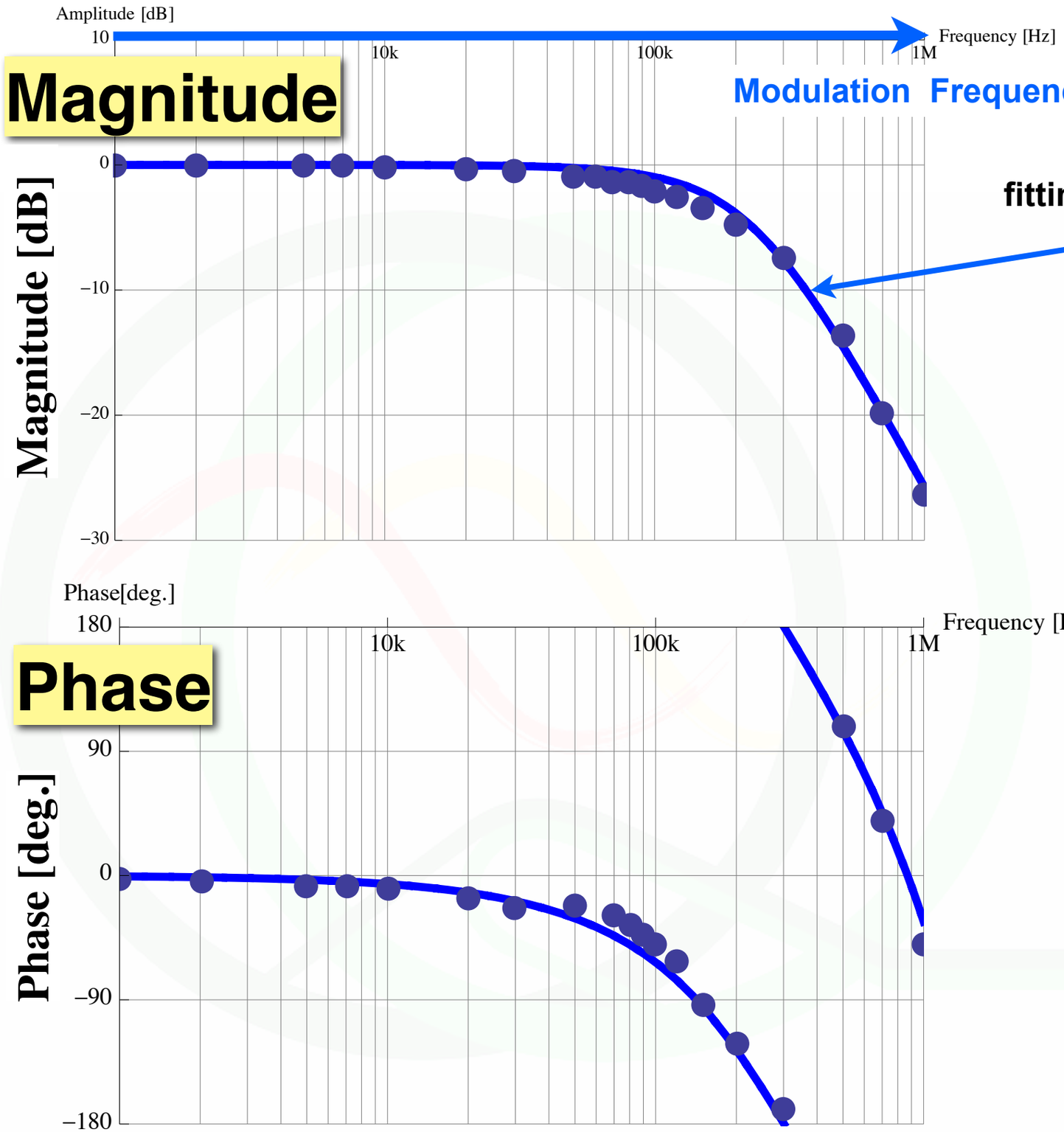
KLY-PLL works successfully,
and the cavity FB control is still normally stable.

w/o KLY-PLL, cavity FB control is broken with oscillation.

High-power test with klystron is not yet done.

Response Property - Klystron Bandwidth (open loop)

Measured Result



T_d : Delay

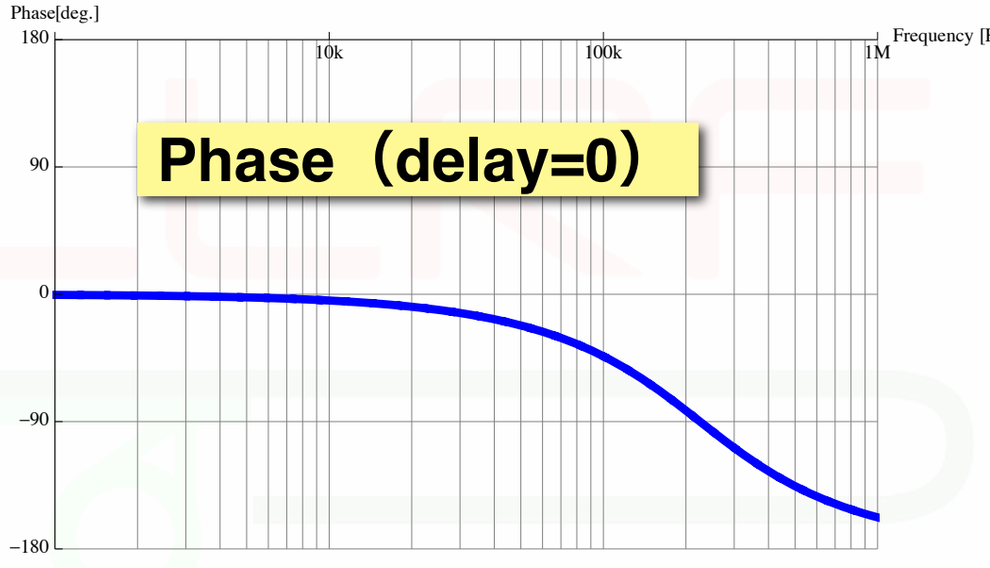
fitting curve with

$$H_{kly}[s] = \frac{1}{1 + s/\omega_{kly} + s^2/\alpha} \cdot e^{-s \cdot T_d}$$

ω_{kly}=130 kHz

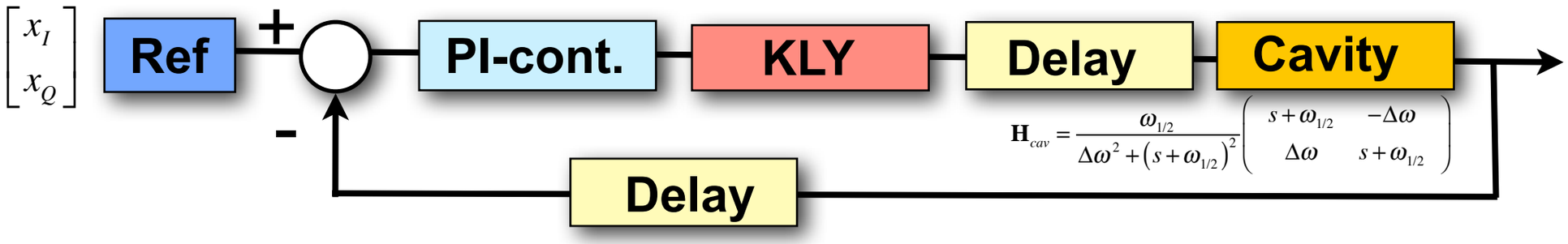
T_d=650ns

$\alpha=2.1\times10^{12}$



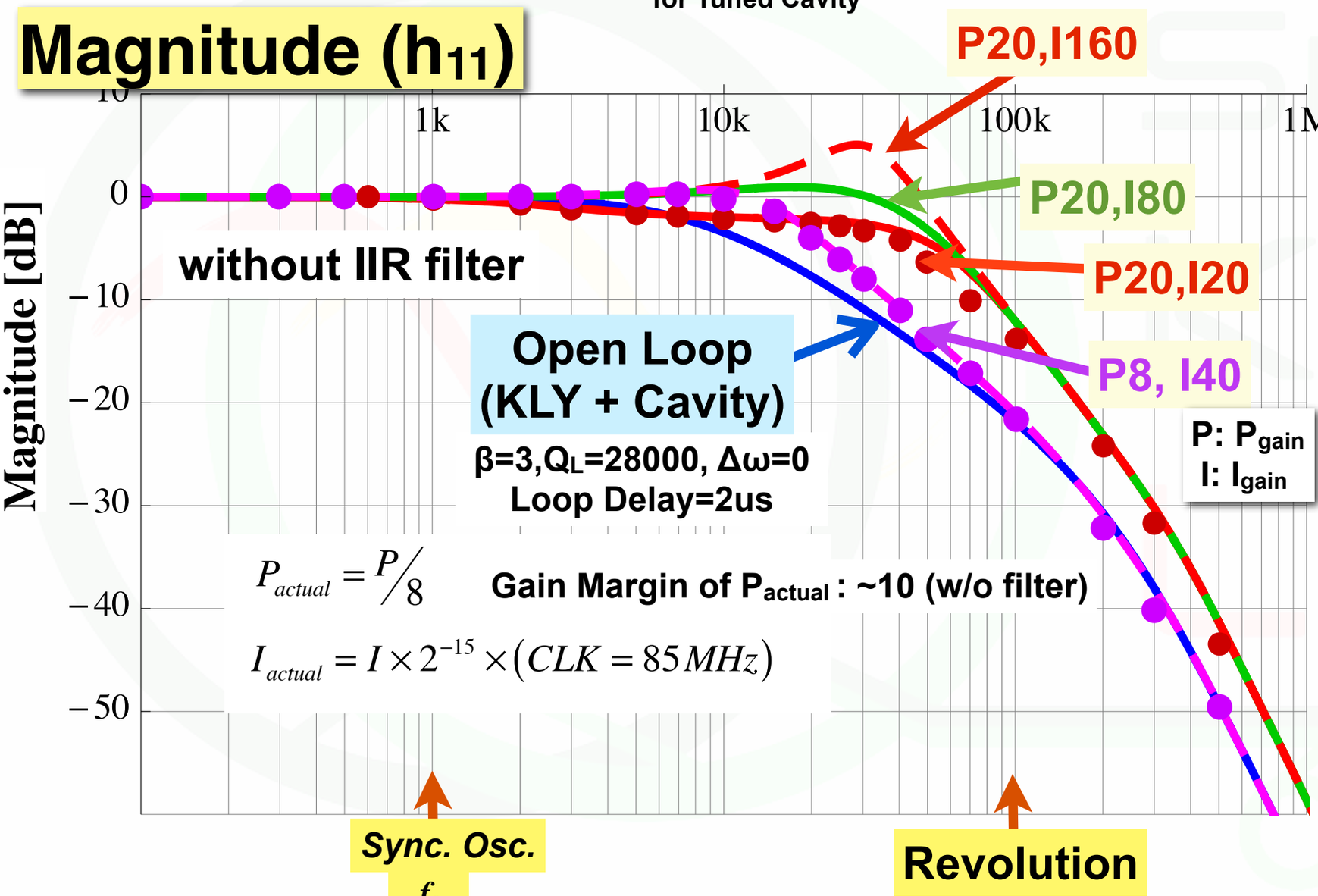
Response Property

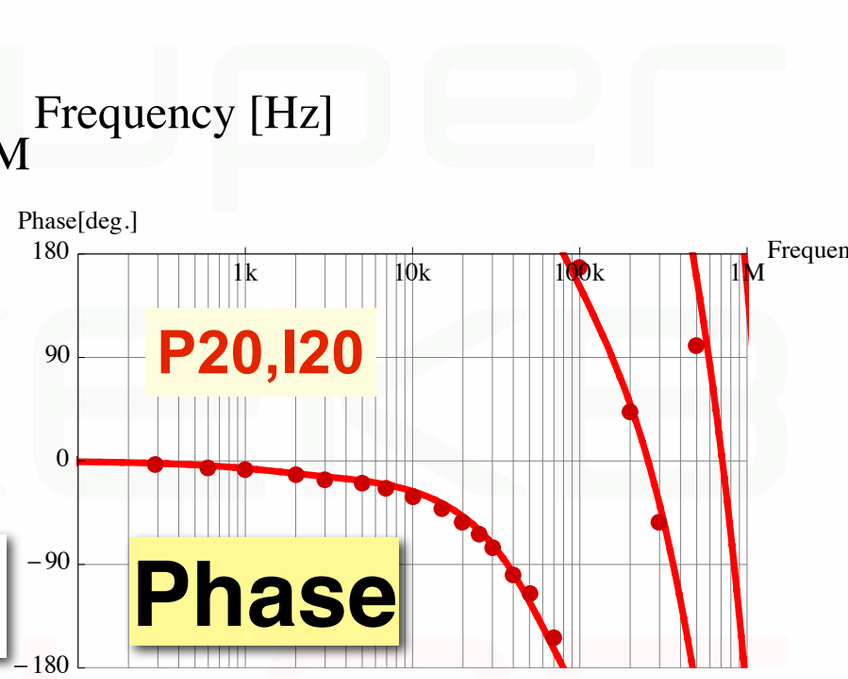
Bode Plot of Closed Loop for ARES

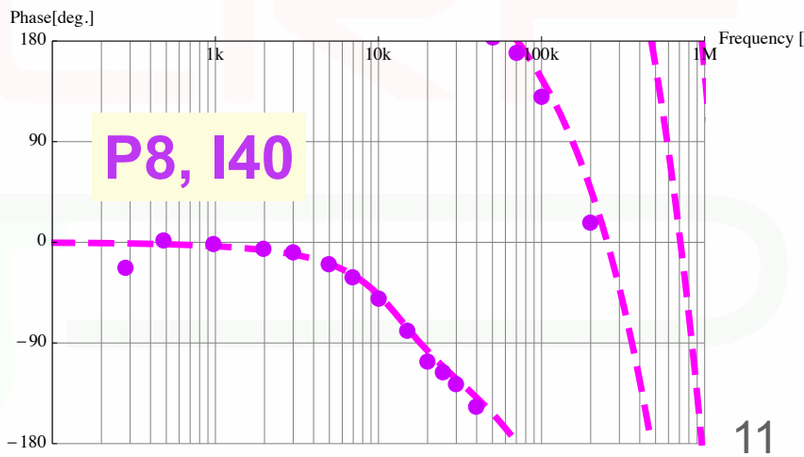


Calculation of Trans. Func. & Measured Result in High Power Test

for Tuned Cavity

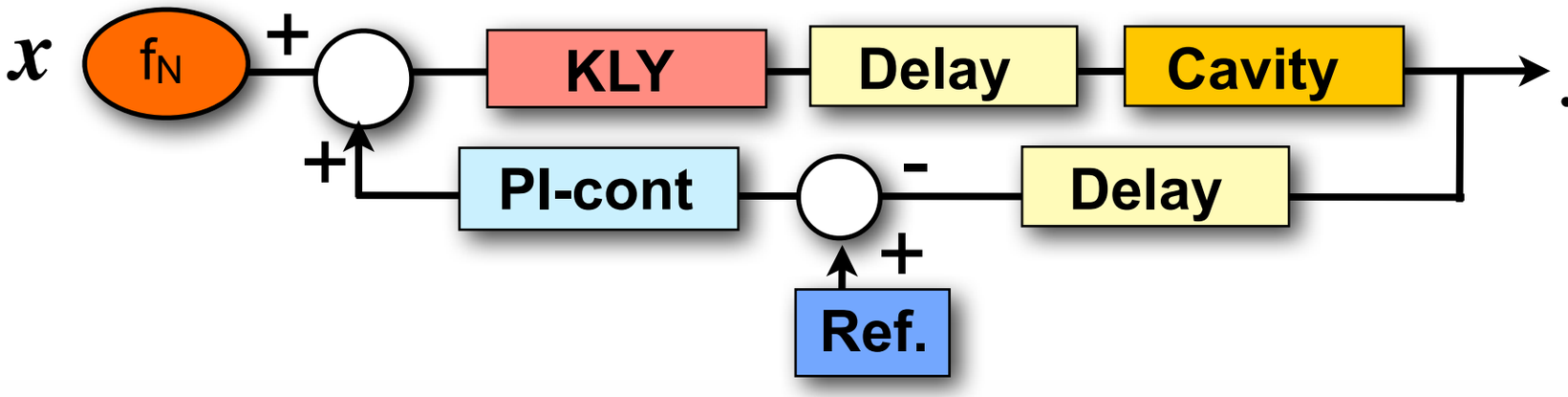






Disturbance Rejection Characteristics

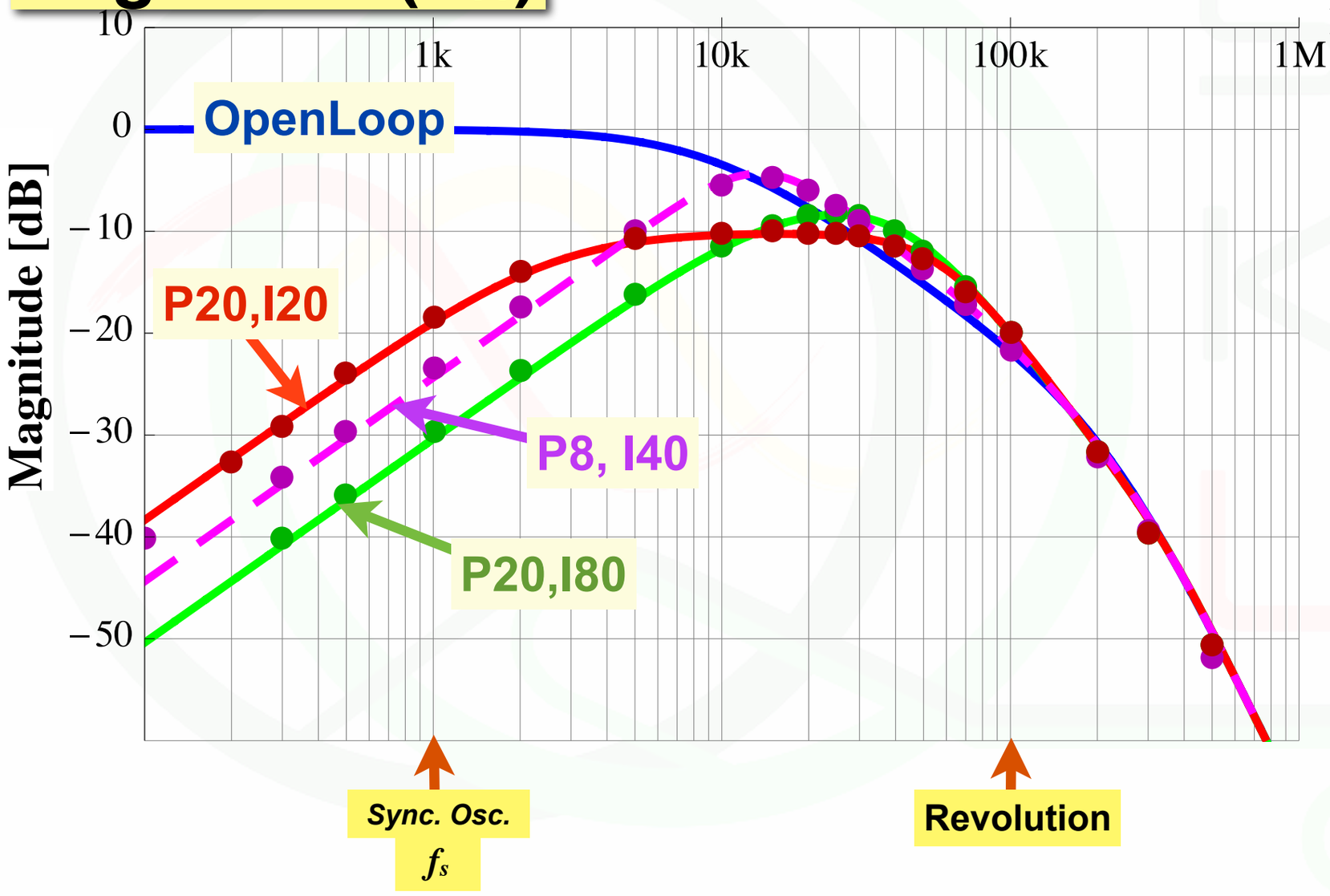
in the closed loop

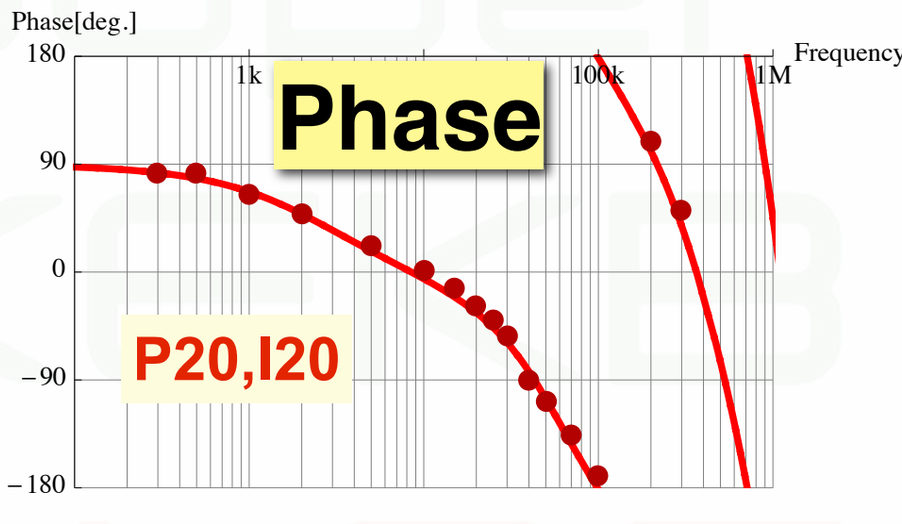


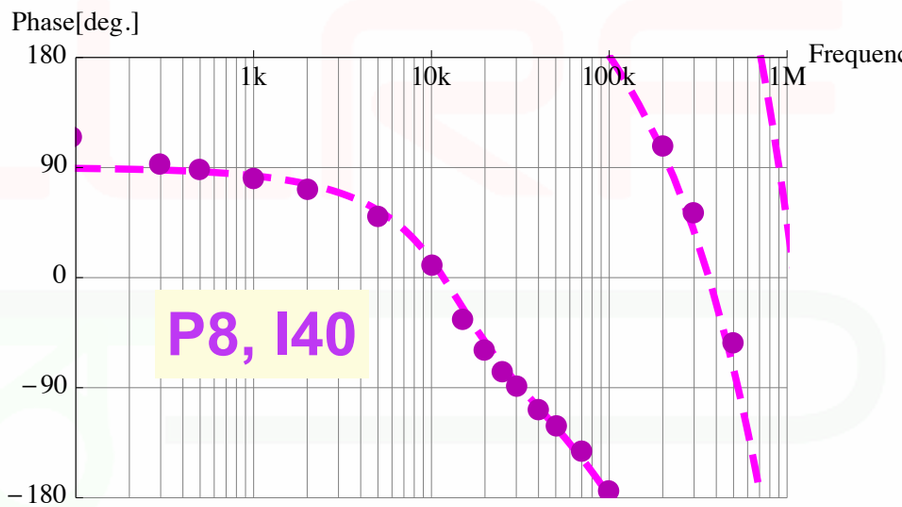
$$y = H[s] \bullet x$$

Magnitude (h_{11})

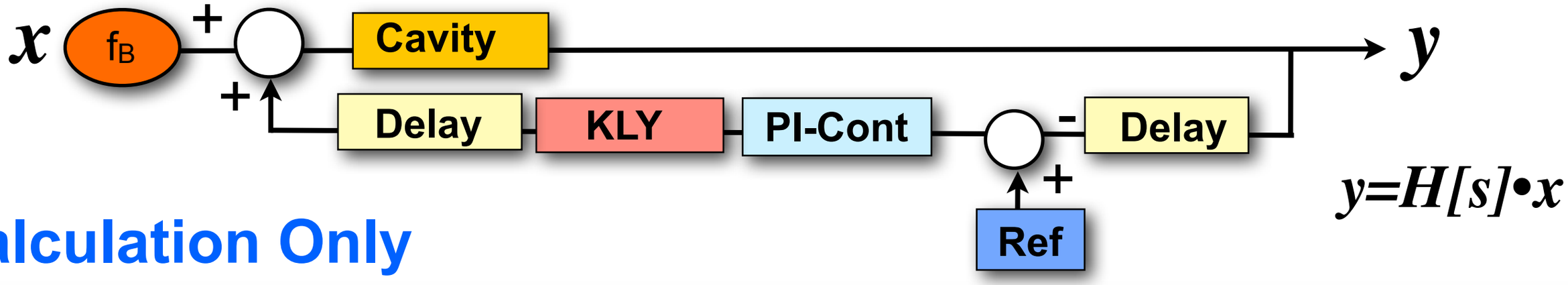
Calculation & Measurement





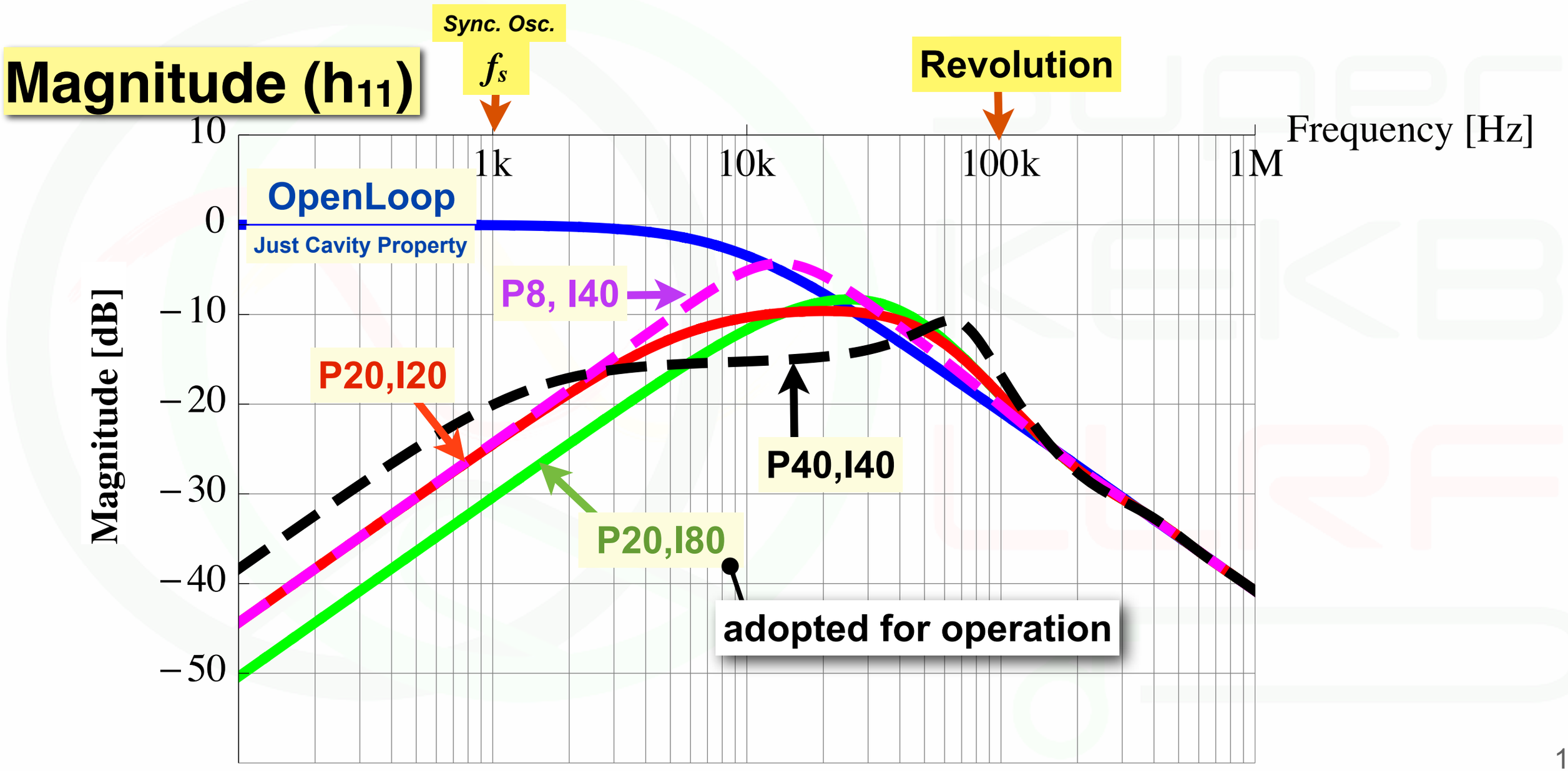


Disturbance Rejection Property for Beam



$y=H[s]\bullet x$

Calculation Only



Simulation of

Phase Modulation due to Bunch Gap (LER)

Time-domain simulation of ARES (LER) for bunch gap transient

Gap 2%

Including 3-cav. structure of the ARES

I_b=3.6 A
(ultimate stage)

Cavity Param.

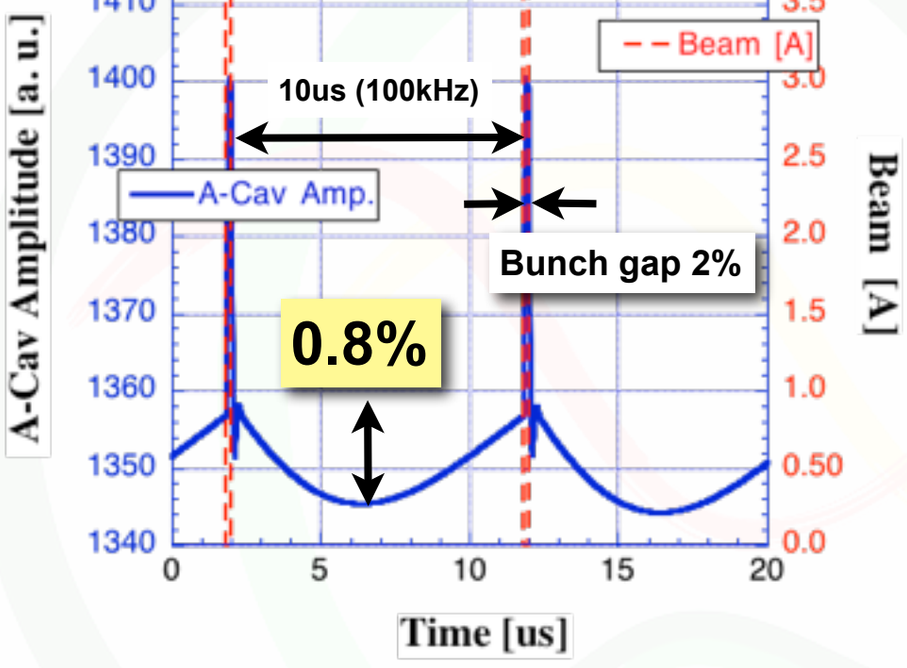
β: 5 , Q_L: 18000 (Q_s=1.6x10^5, Q_c=50, Q_a=2.5x10^4)
P_c: 140 kW , P_b: 460 kW
Φ_{acc}: 74.5 deg.
A-cav detuning: -280 kHz

FB Param.

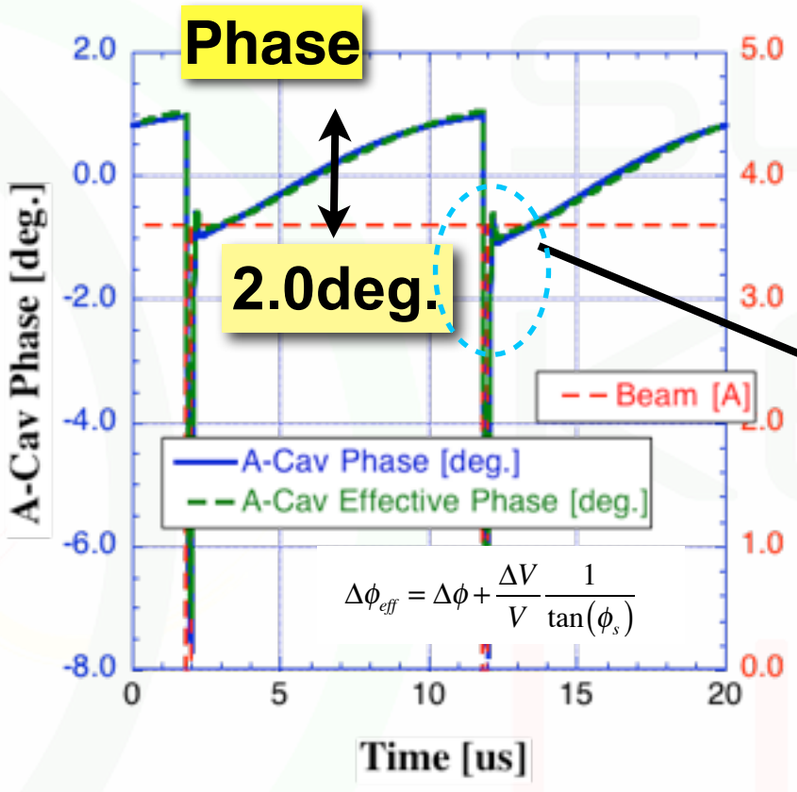
P_{gain}: 20 (P_{actual}=2.5)
I_{gain}: 80 (I_{actual}=2x10^5)
Loop delay: 2 us

KLY band : 100 kHz

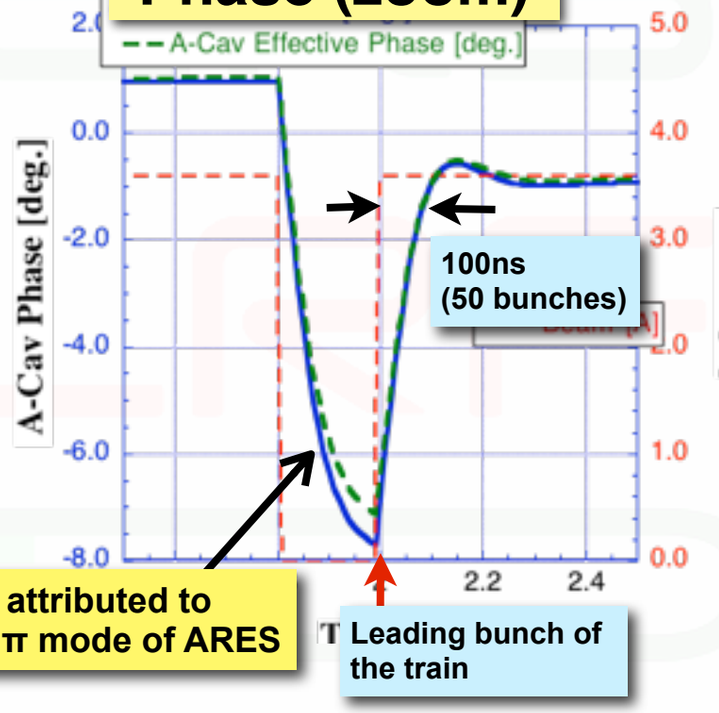
Amplitude



Phase



Phase (zoom)



agree well with

$$\frac{\Delta V}{V_c} = \frac{\omega_{rf}}{2V_c}\left(\frac{R}{Q}\right) I_b \Delta t \cdot \tan\phi_s \qquad \Delta\phi = \frac{\omega_{rf}}{2V_c}\left(\frac{R}{Q}\right) I_b \Delta t$$

FB-control effective is small against gap transient. (almost cavity response)

FF-control compensation is impossible (Bandwidth of >1MHz is needed).

KLY-BW is ~100kHz

Simulation of

Phase Modulation due to Bunch Gap (HER)

Time-domain simulation of SCC & ARES for HER bunch gap transient

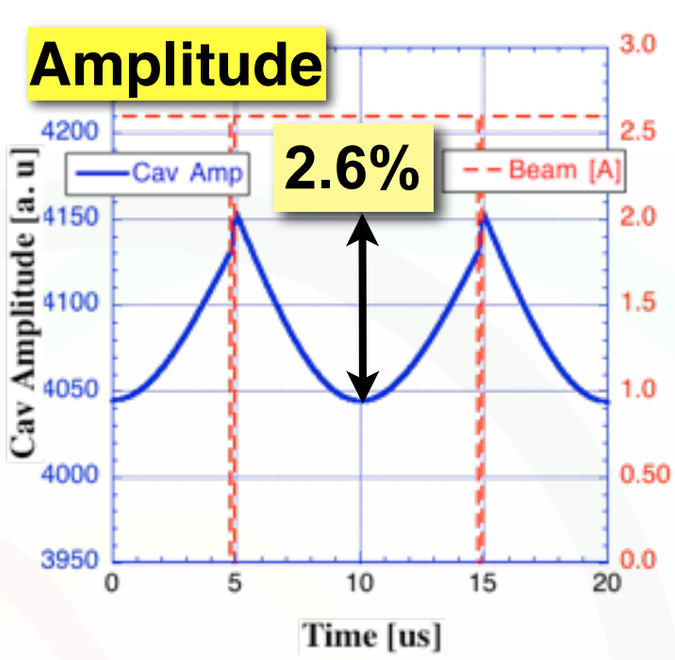
HER : I_b=2.6 A
(ultimate stage)

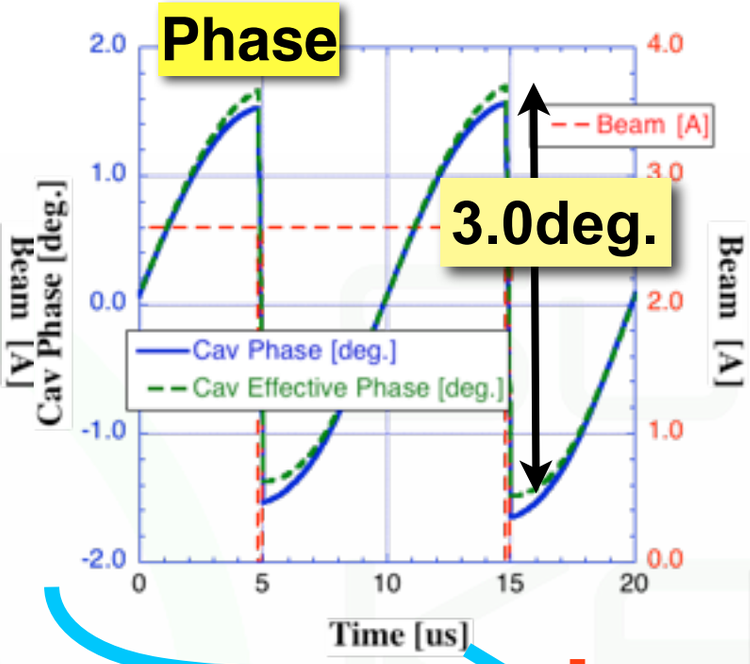
Gap 2%

SCC

Q_0:1e9, Q_L: 50000
V_c: 1.5MV
P_b: 600 kW
Φ_{acc}: 84 deg.
Detuning: -44 kHz

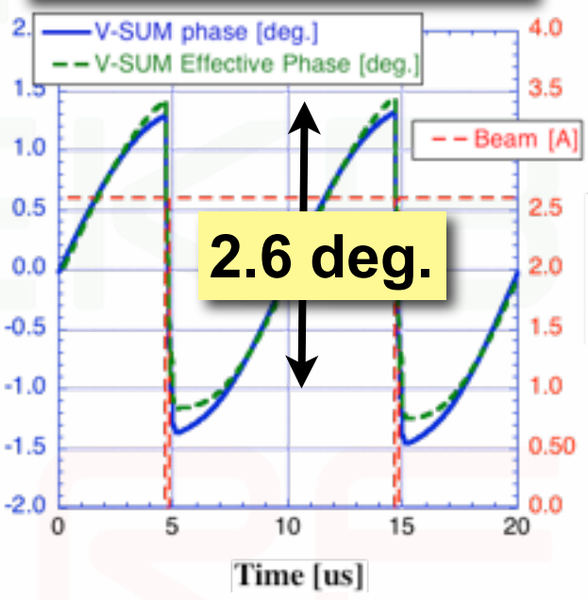
P_{gain}: 800 (100)
I_{gain}: 4000 (10^7)
Loop delay: 2 us





8xARES (0.5MV)
+
8xSCC (1.5MV)

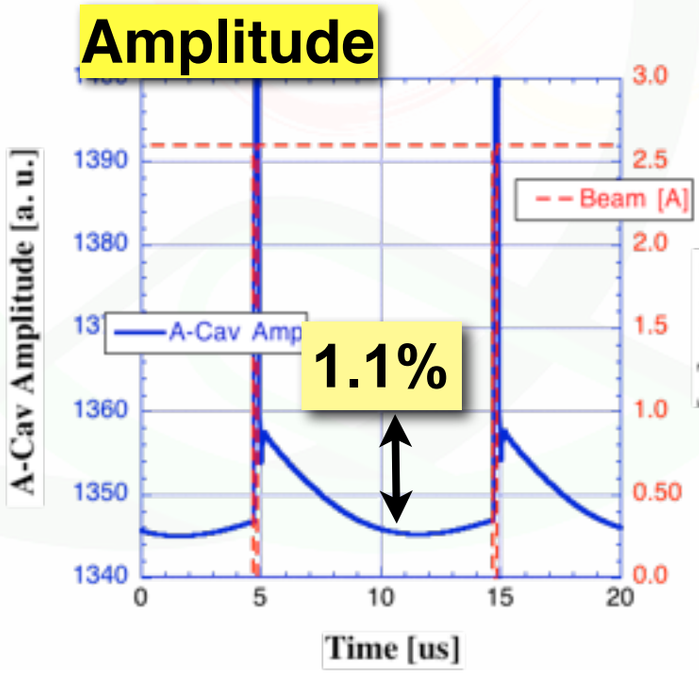
Vector SUM of V_c Phase Shift

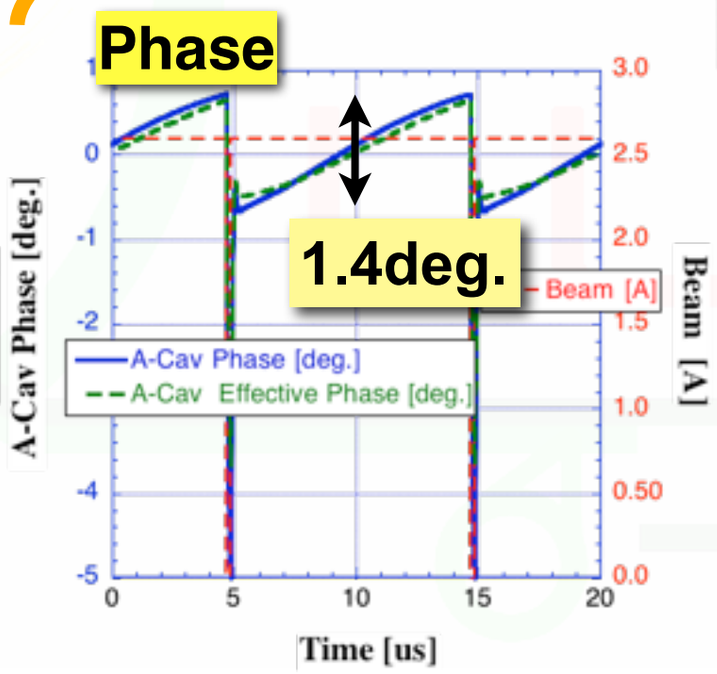


ARES

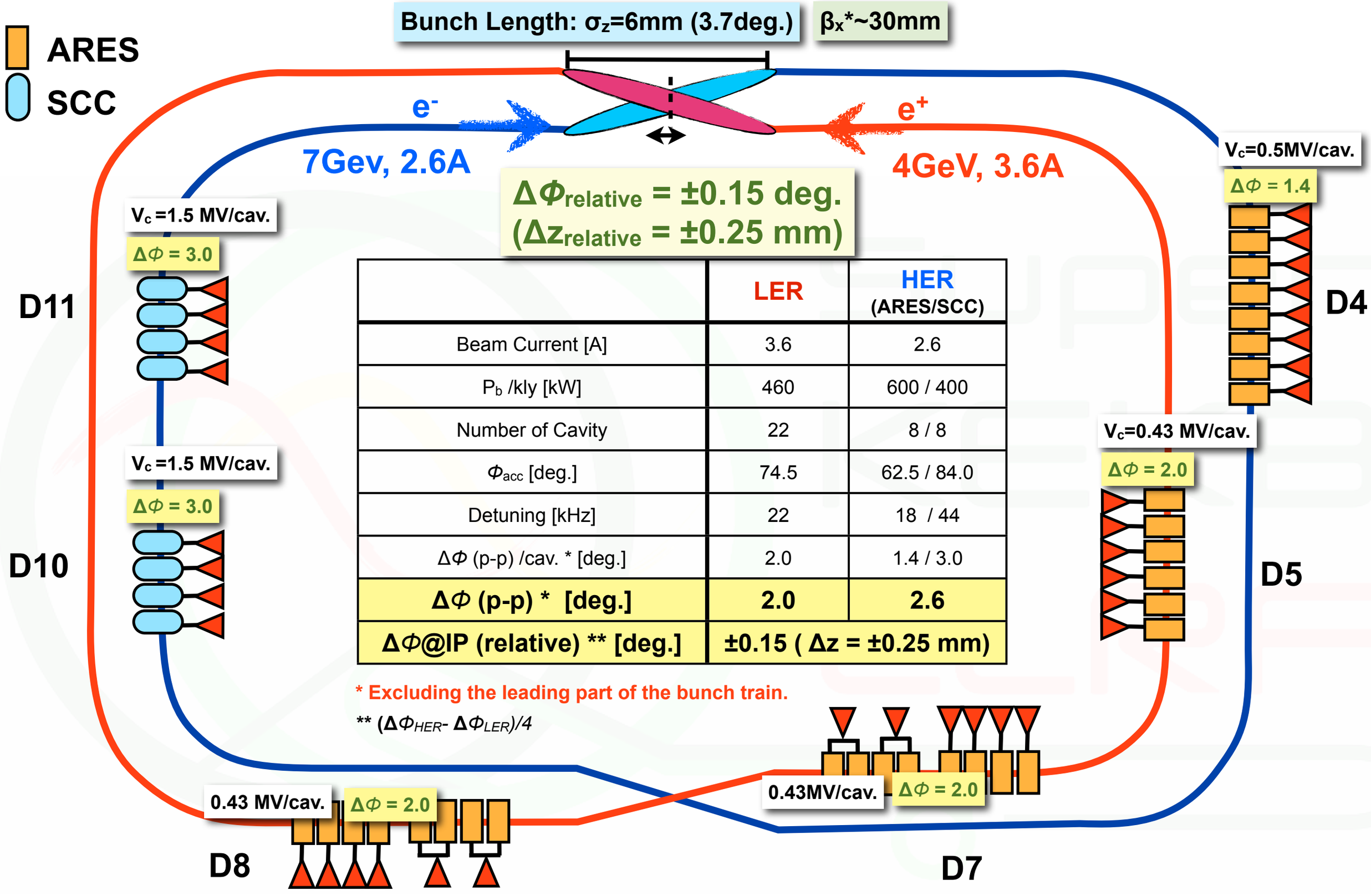
β: 5 , Q_L: 18000
Pc: 150 kW
P_b:600 kW
Φ_{acc}: 62.5 deg.
Detuning: -180 kHz

P_{gain}: 20 (2.5)
I_{gain}: 80 (2x10^5)
Loop delay: 2 us





Estimation of Relative Phase Shift@IP between HER & LER due to 2%-bunch gap in the ultimate stage



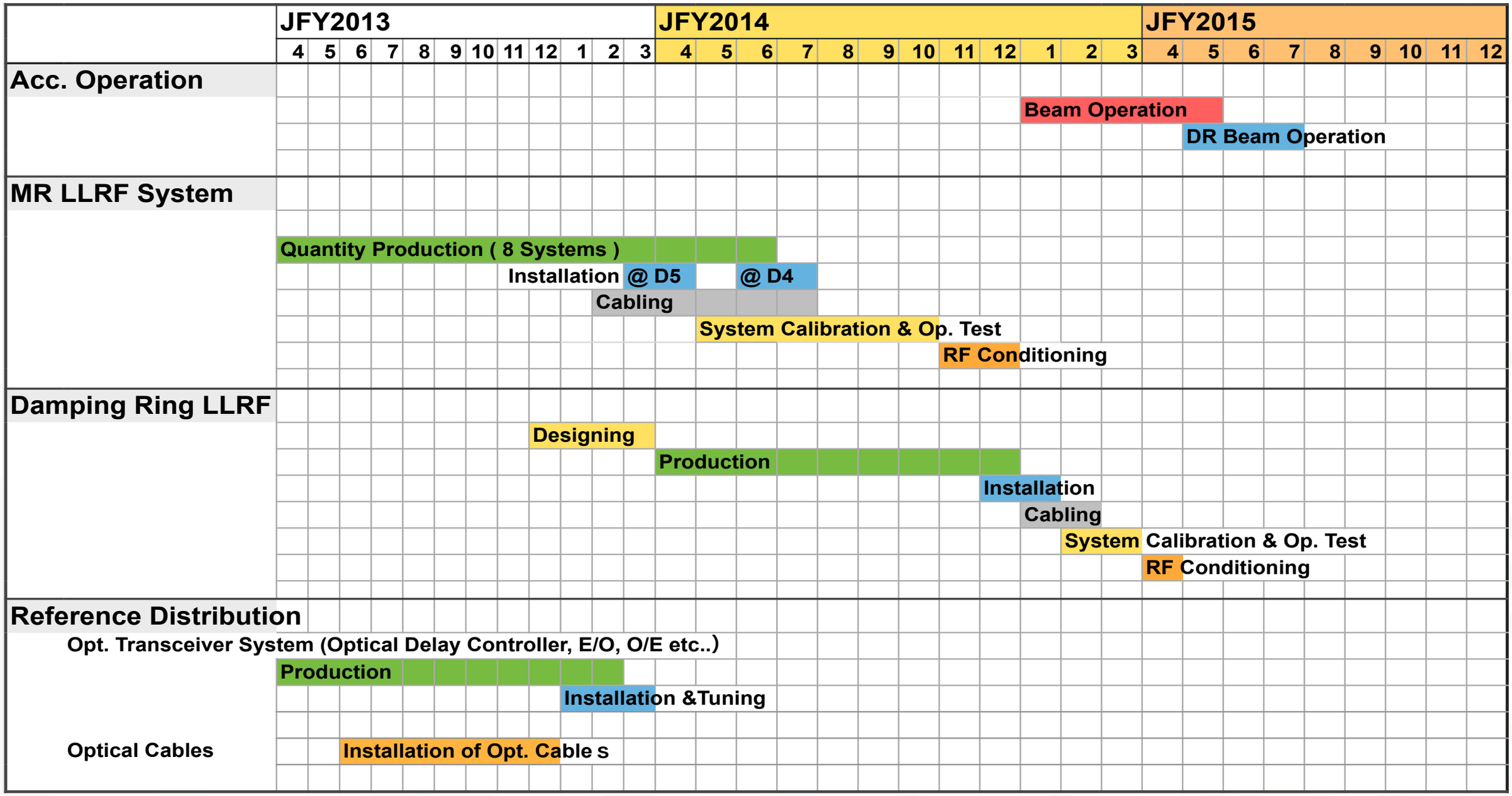
	LER	HER (ARES/SCC)
Beam Current [A]	3.6	2.6
P_b /kly [kW]	460	600 / 400
Number of Cavity	22	8 / 8
Φ_{acc} [deg.]	74.5	62.5 / 84.0
Detuning [kHz]	22	18 / 44
$\Delta\Phi$ (p-p) /cav. * [deg.]	2.0	1.4 / 3.0
$\Delta\Phi$ (p-p) * [deg.]	**2.0**	**2.6**
$\Delta\Phi$@IP (relative) ** [deg.]	**±0.15 (Δz = ±0.25 mm)**	

* Excluding the leading part of the bunch train.

** $(\Delta\Phi_{HER} - \Delta\Phi_{LER})/4$

Schedule of Production and Installation

*based on the original schedule for the operation.



- Mass production of 8 systems is now in progress for D4&D5, and will be installed on March and June in this year.
- RF conditioning is scheduled in November & December JFY2014.
- DR-LLRF designing has been completed, and the production will be JFY2014.

Summary

- Now the mass production of new LLRF system is in progress on schedule. They will be applied at D4 and D5 sections.

- Newly klystron phase lock loop was implemented in the FPGA, and successfully worked. But high power test is not yet.

- RF phase modulation due to the bunch gap transient was estimated. The relative phase shift between both rings at IP is expected to be acceptably small. However, large-phase displacement appears at the leading part of the bunch train.

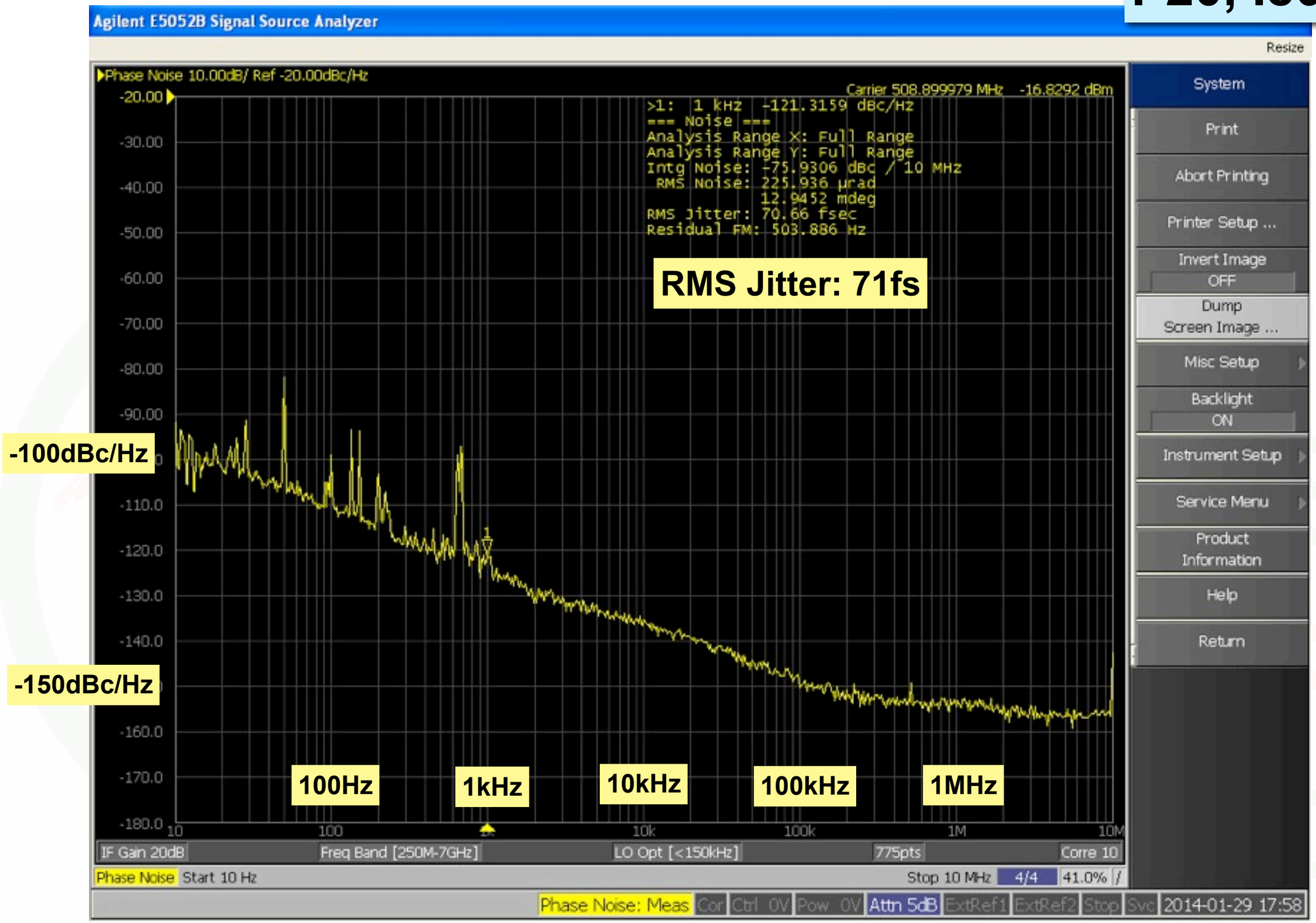
- DR-LLRF system will be produced next JFY.

Thank you for your attention !

Followed by Backup Slides

SB Phase Noise of ARES under FB control.

P20, I80



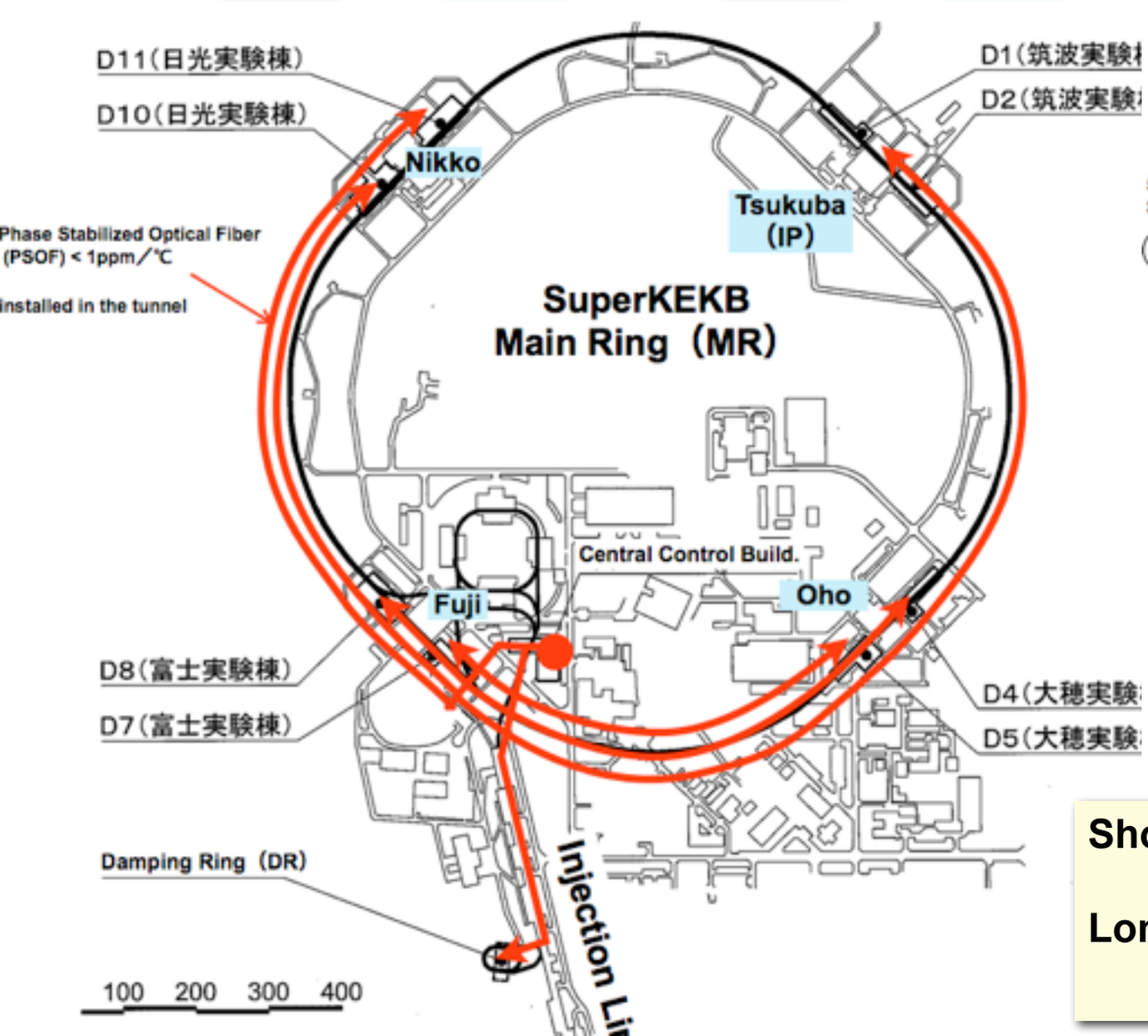
RF Reference Distribution

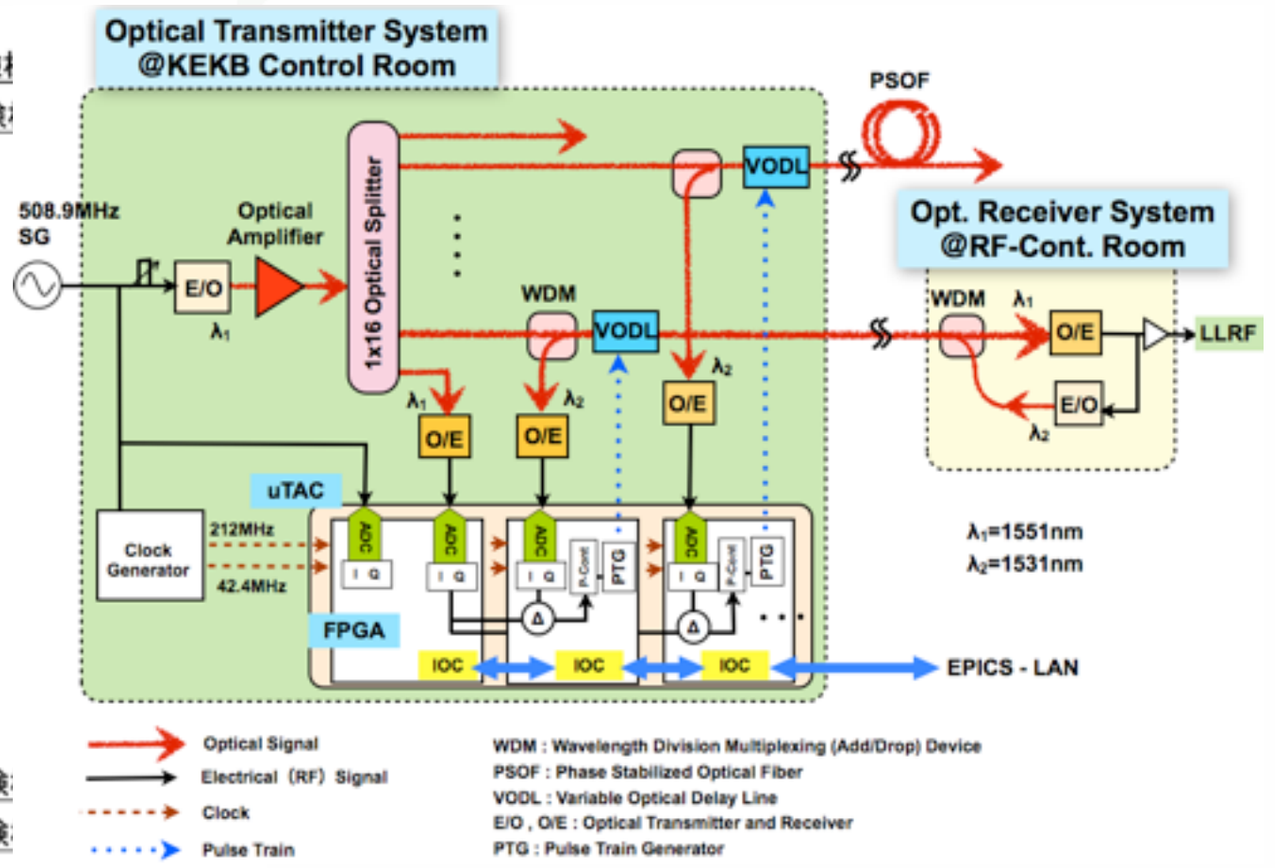
Features

- Optical distribution by means of “Star” configuration from the central control room (CCR).
- “Phase Stabilized Optical Fiber (PSOF)”, which has small thermal coefficient, is adapted : < 1ppm/°C (5 ps/km//°C)
- Furthermore, optical delay control of thermal drift compensation is applied at CCR for all transfer lines.
- The optical transceivers (E/O and O/E) are the same as J-PARC Linac; They have practical accomplishment of seven-year operation, quite low jitter and high thermal stability with Pertie device.

Status

- Installation of the PSOF cables to all RF sections and Tsukuba-B3 was completed.
- Optical transceivers and the drift compensation system will be install in this month.
- Connection into the electronics hut of the Belle-II and extension to the DR will be done this year (next JFY).

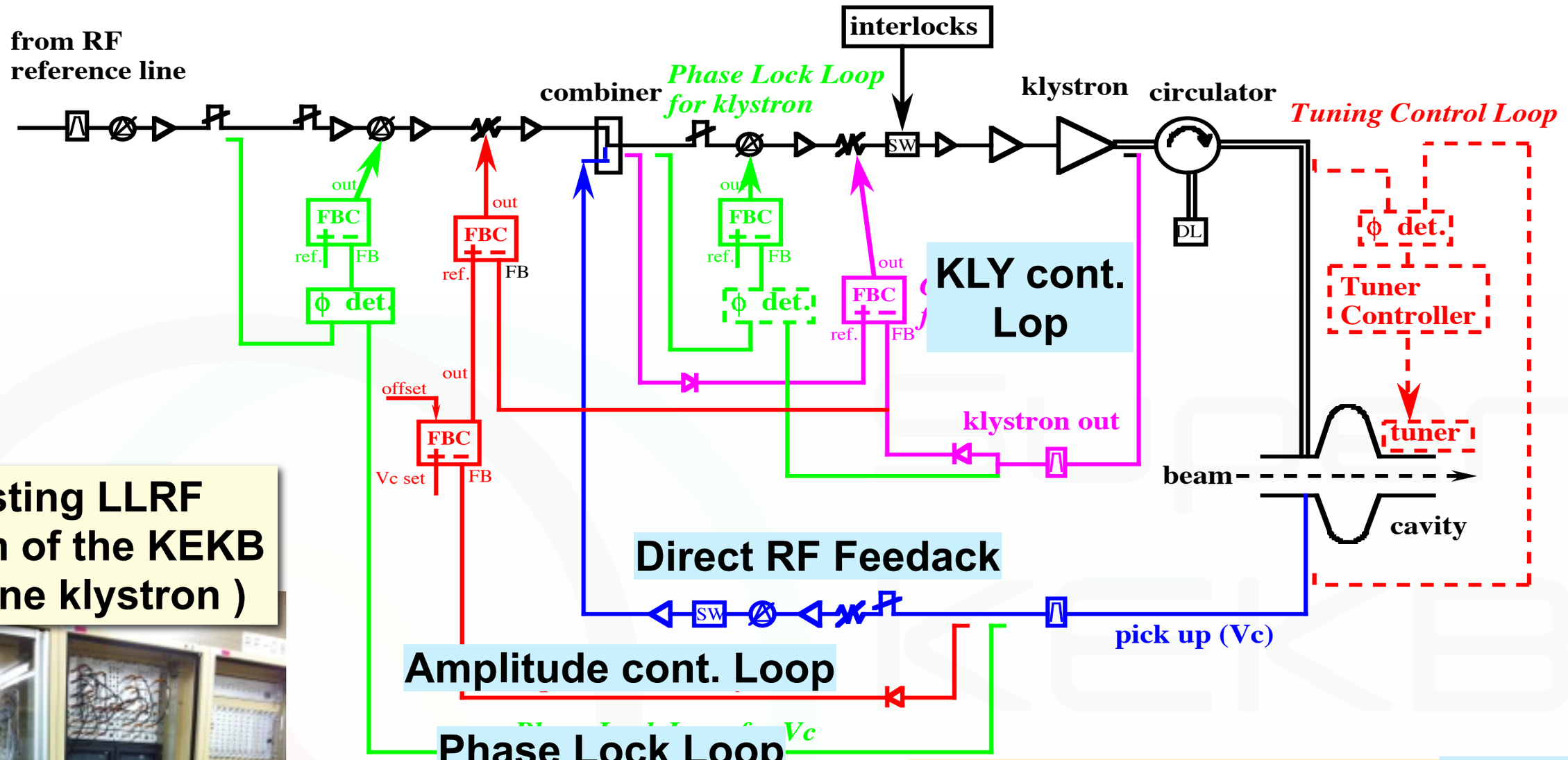




Short term stability (time jitter) : ~0.1 ps (rms)

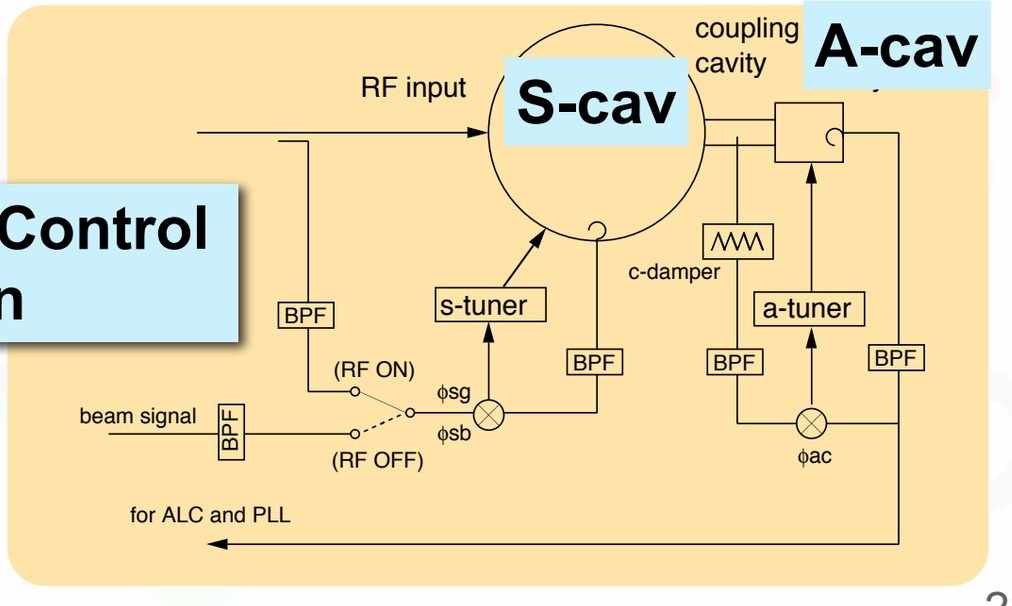
Long term stability (pk-pk) : ±0.1° @508.9MHz = ±0.55 ps with the optical delay control.

KEKB-LLRF System



Existing LLRF System of the KEKB (for one klystron)

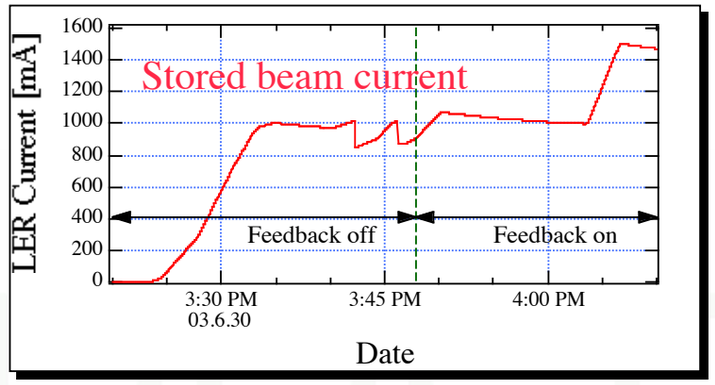
ARES Tuner Control Configuration

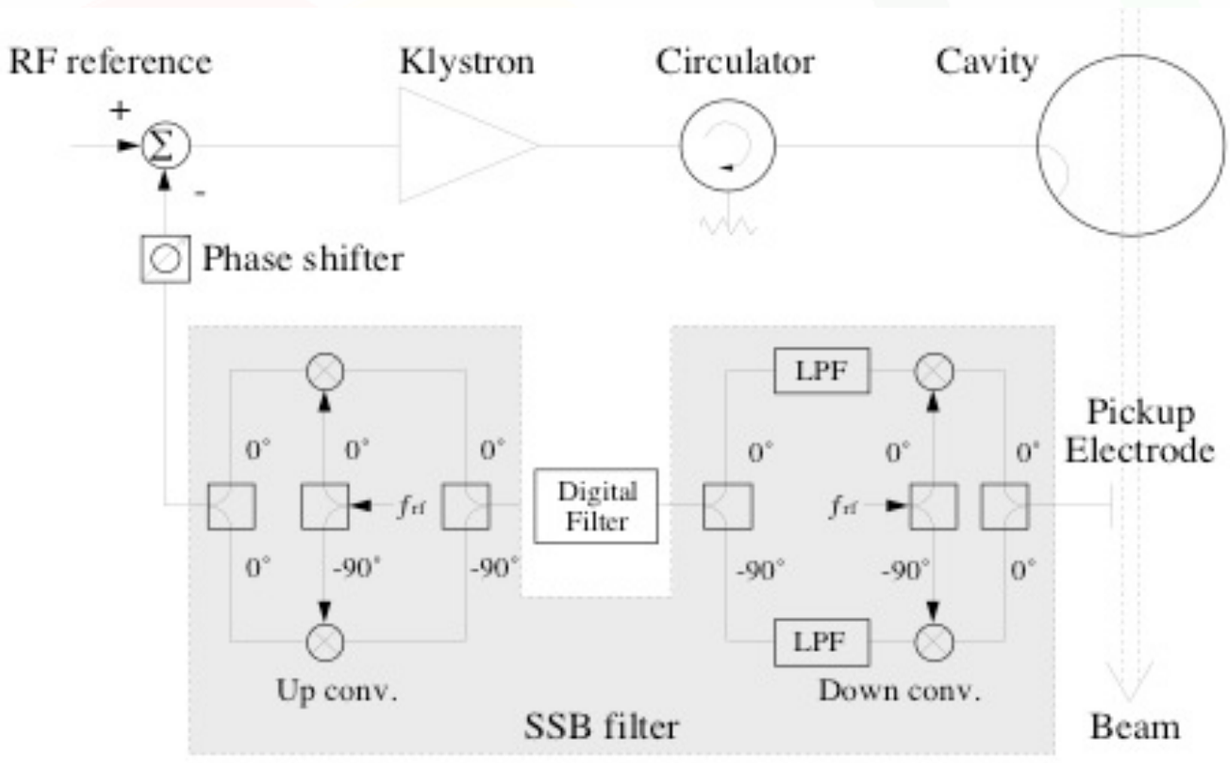


The -1 mode feedback

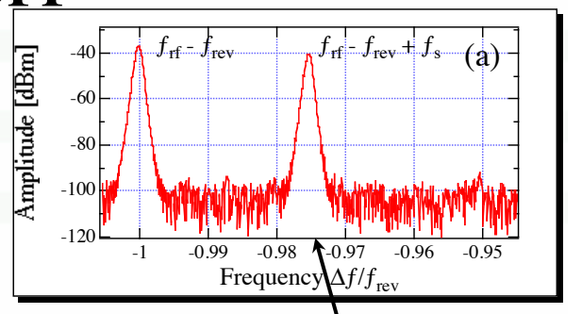
In the KEKB Operation

- **Beam current was limited due to the -1 mode instability at 1 A in LER and 1.2 A in HER, much lower current than expected.**
- **The -1 mode digital feedback selectively reduces impedance at the driving frequency.**
- **After the -1 mode feedback was installed, the beam current could be successfully increased.**





FB OFF



-1 mode sideband

FB ON