Timing Control

Hitoshi Sugimura

Outline

- **Construction of DR Sub Timing Station**
  - Fixed charging time delivery to injection/extraction kicker magnet.
- **Beam Gate via "Distributed bus"**
- **Optional Extraction System**
  - Extraction after dispersion measurement.
  - Beam Extraction at DR after LER Abort.

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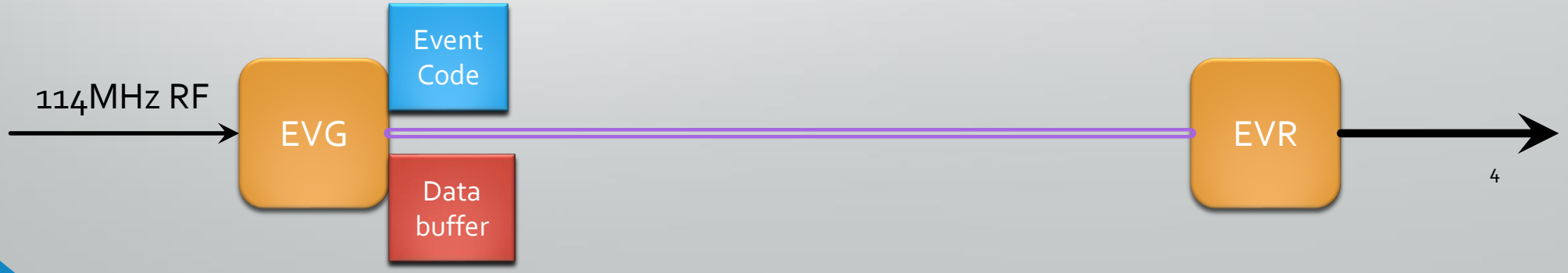
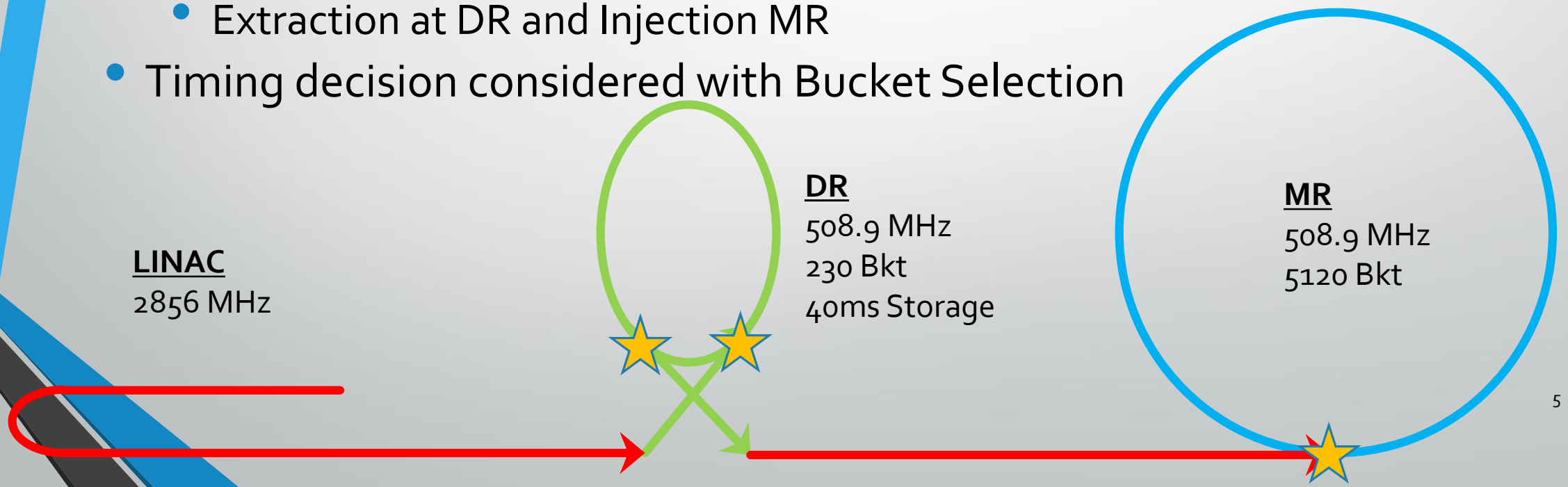
Event Timing System

- We built up timing delivery structure by using a pair of Event Generator(EVG) and Event Receiver(EVR) series produced by MRF/SINAP.
- 2-byte of characters are transmitted from EVG to EVR synchronized with 114 MHz event clock cycle.
- First 8-bit is Event Code and the second 8-bit is shared with Data buffer and Distributed Bus.

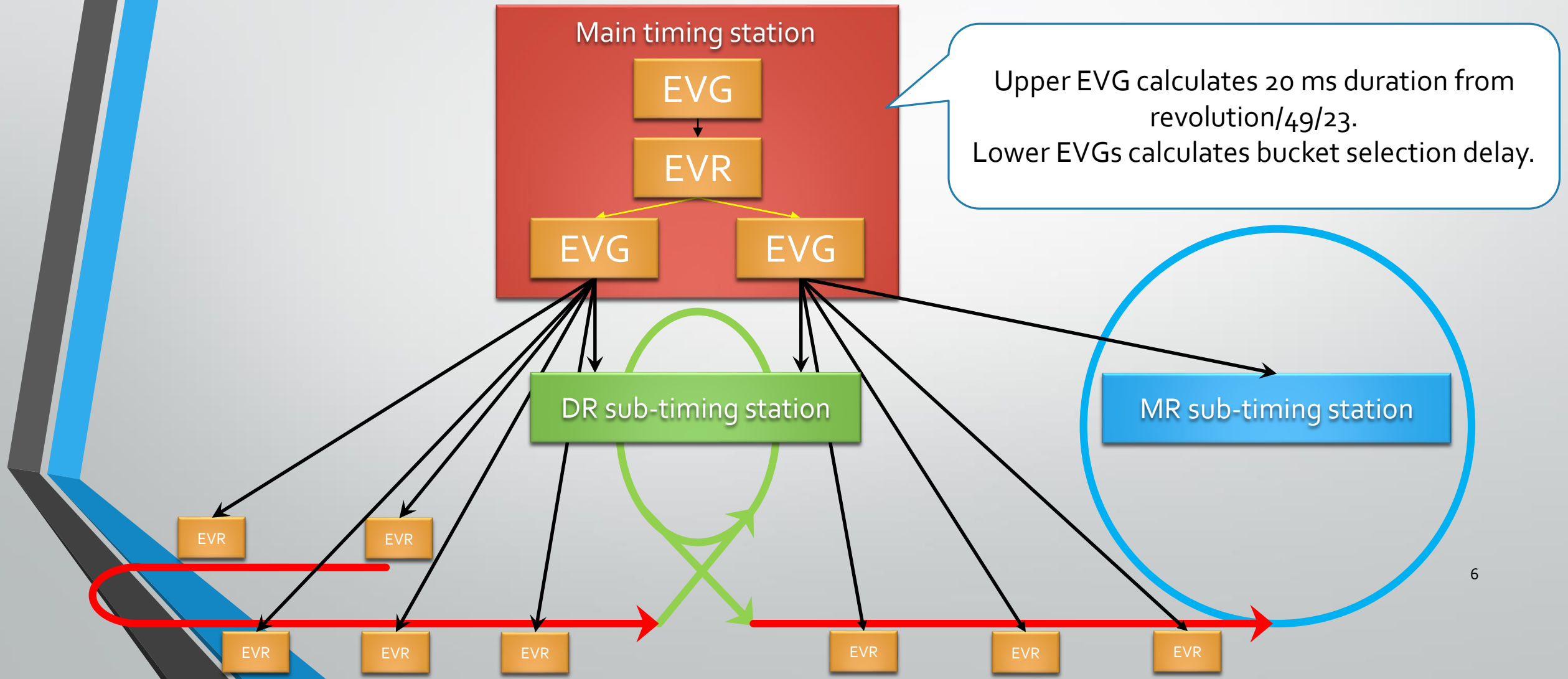


Construction of Timing Station at LINAC/DR/MR

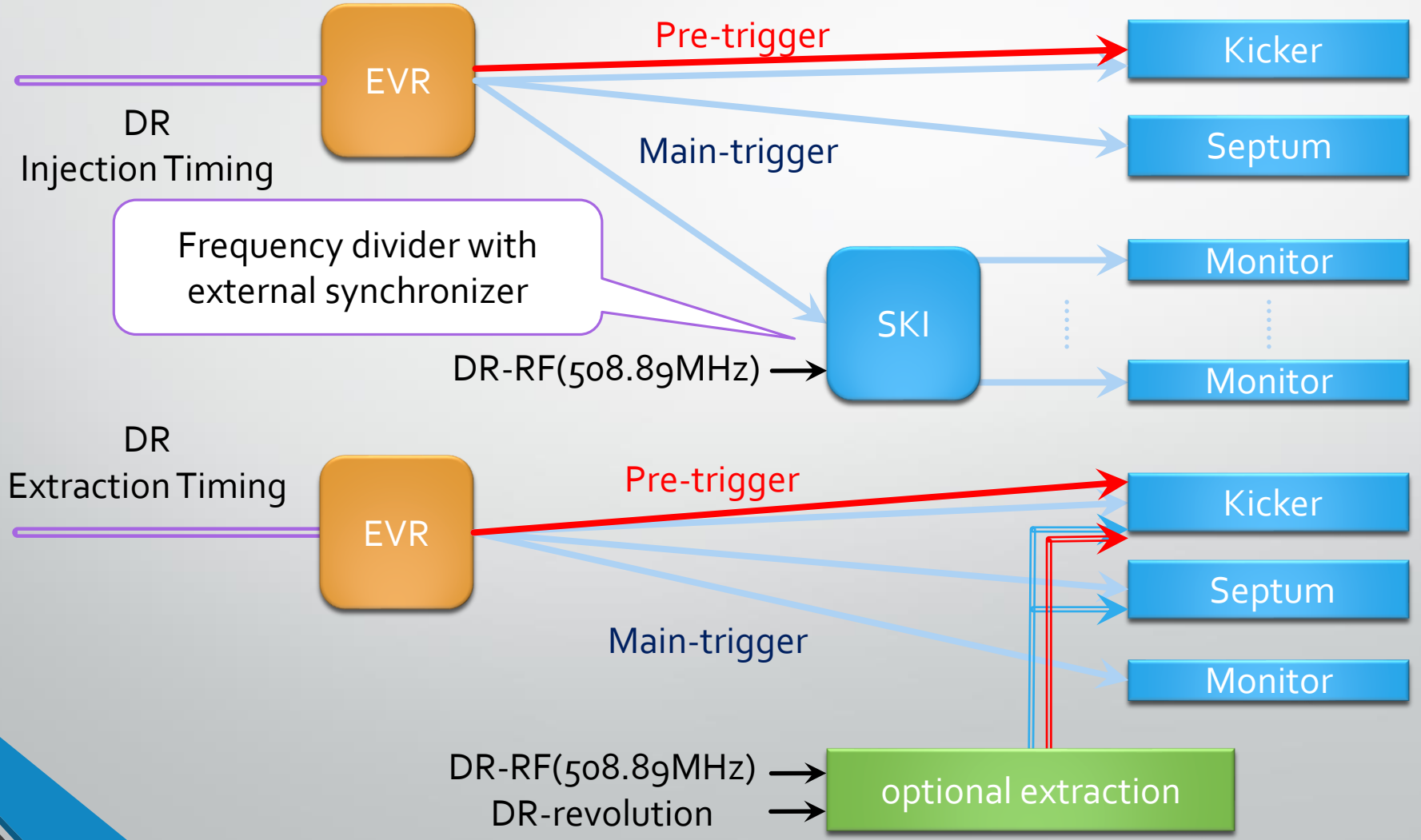
- Without DR, One timing is enough. But With DR …
- Two timing is needed to consider about DR storage
  - Injection at DR
  - Extraction at DR and Injection MR
- Timing decision considered with Bucket Selection



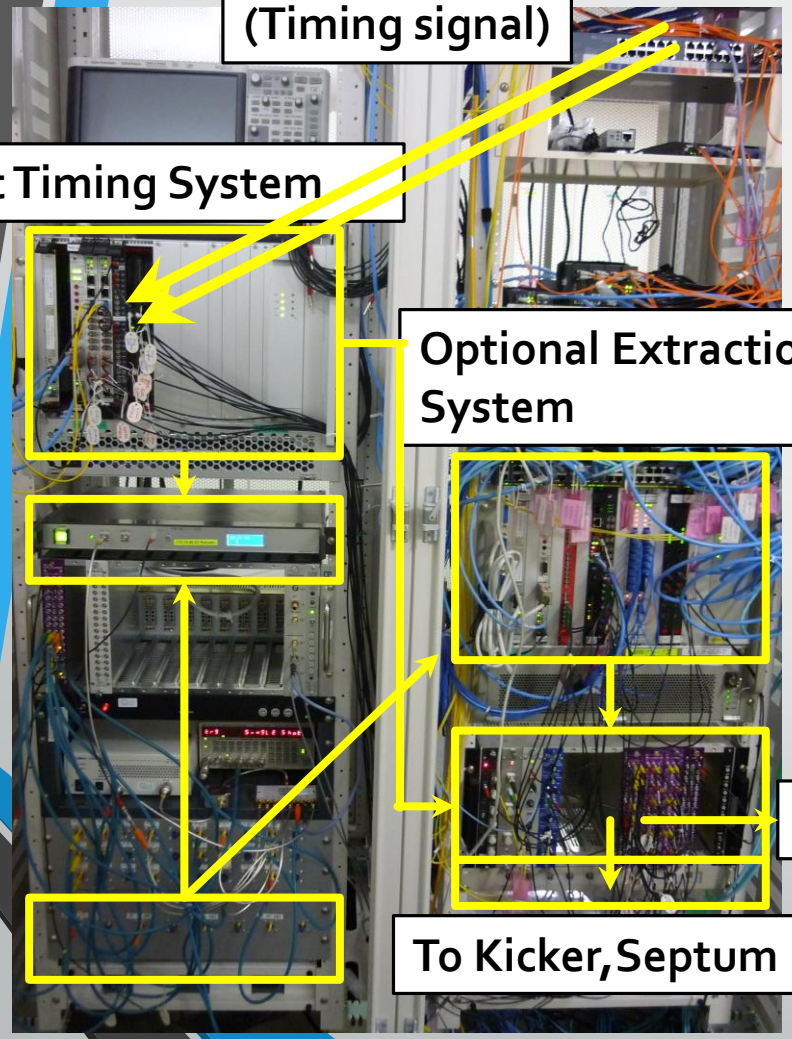
Construction of Timing Station at LINAC/DR/MR

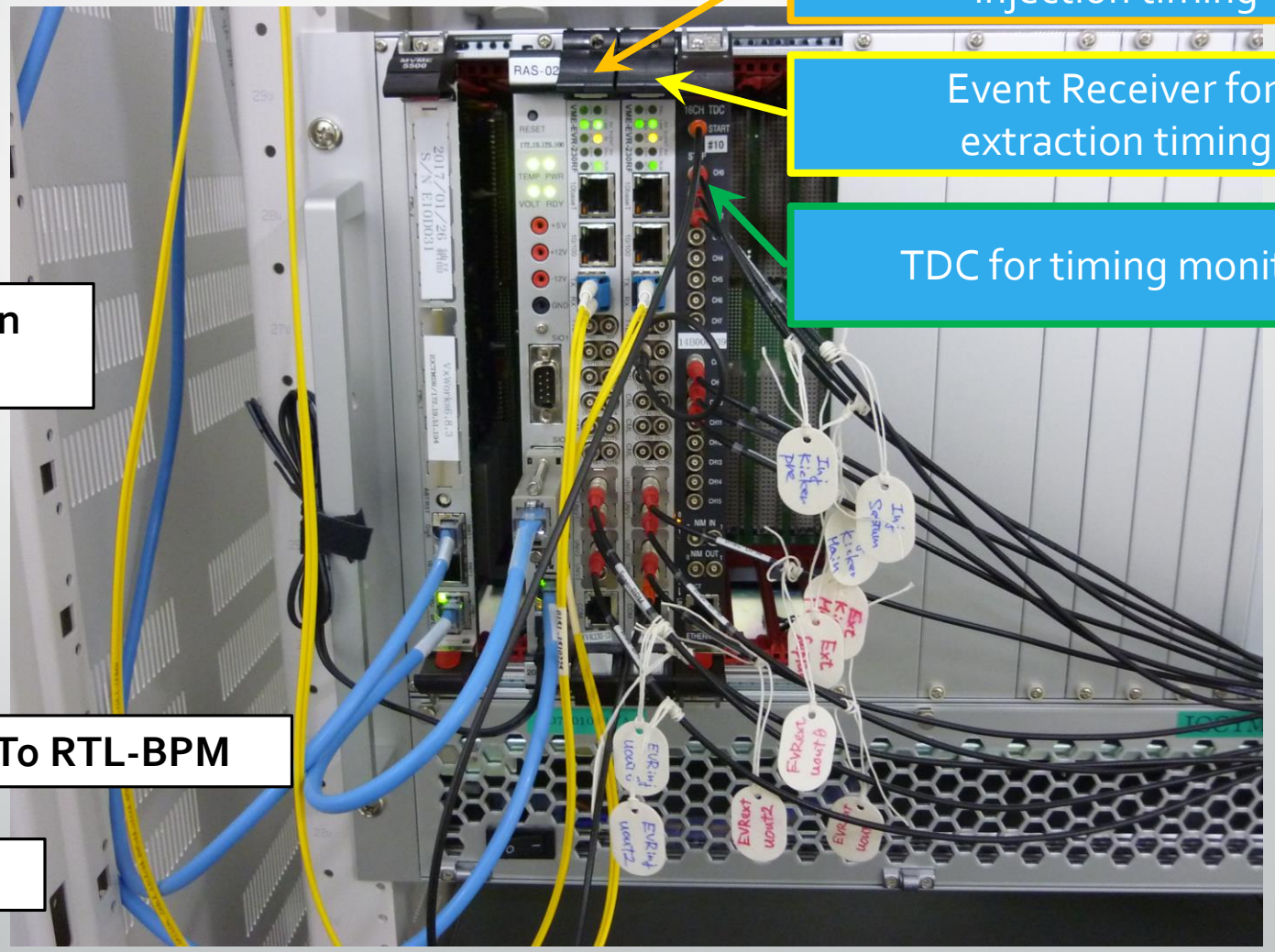


Construction of DR Sub timing Station (2017.7-)

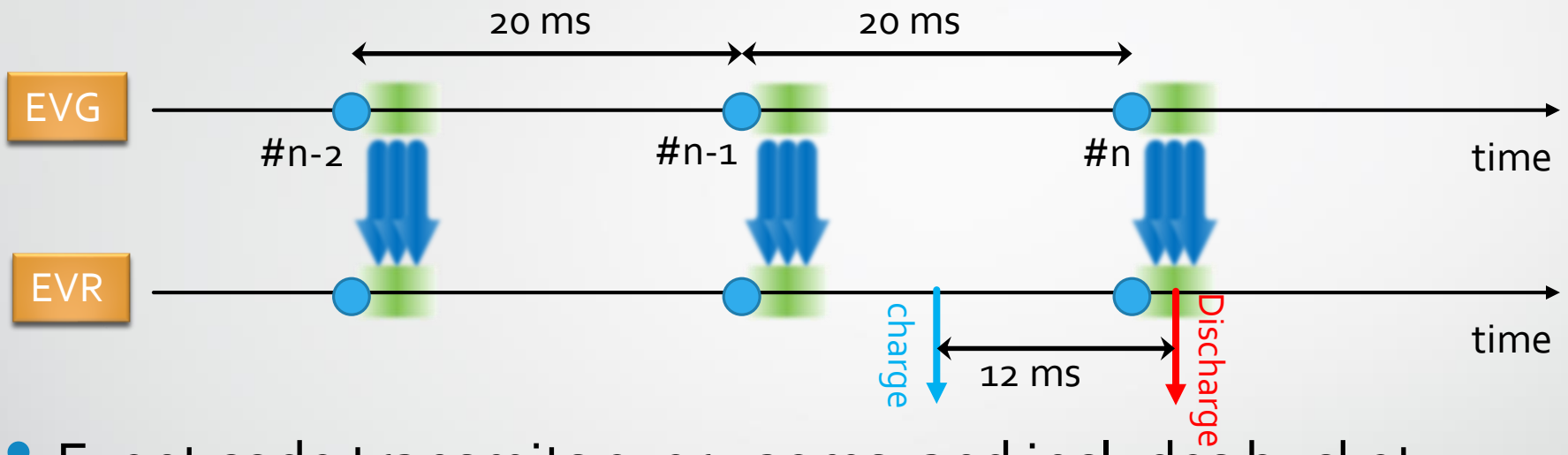


Construction of DR Sub timing Station (2017.7-)



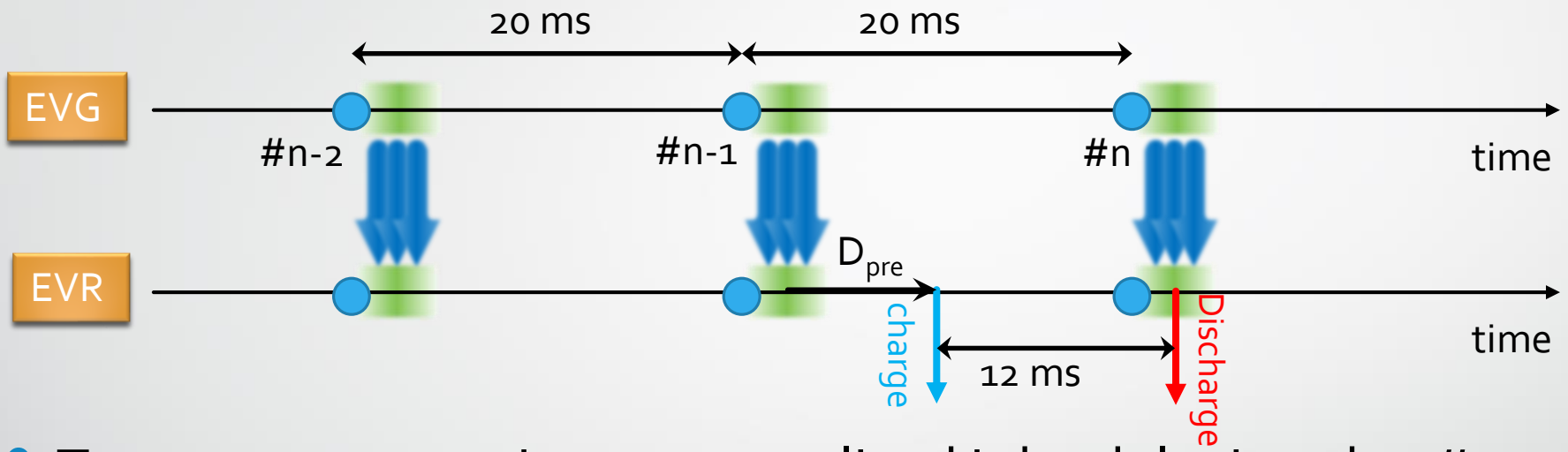


Pre-Trigger generation with fixed time duration for Kicker magnets



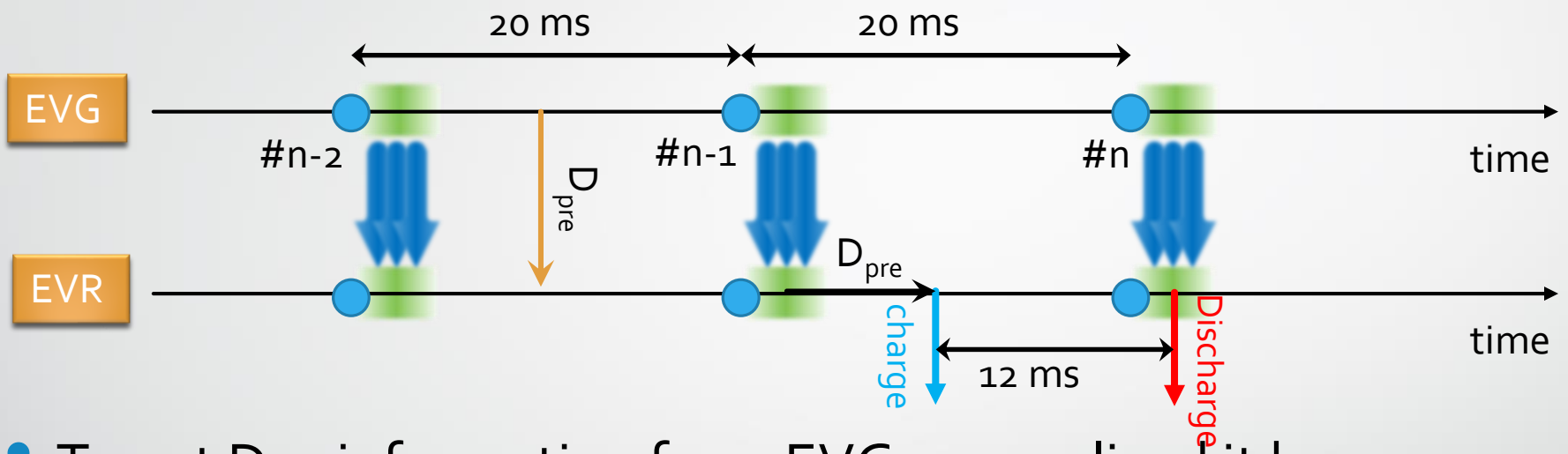
- Event code transmits every 20ms, and includes bucket selection delay within 2ms. Timing is fluctuated.
- Trigger timing to charge Kicker magnet has to send 12 ms before discharge timing.
- If discharge timing generates at shot #n, charge timing(pre-trigger) has to generate between shot #n-1 and #n

Pre-Trigger generation with fixed time duration for Kicker magnets



- To generate pre-trigger, we realized it by delaying shot#n-1 timing.
- The delay time (D_{pre}) must be considered with bucket selection delay otherwise time duration of 12 ms is fluctuated.
- The value of Dpre is represented by follows formula.
  - **Dpre = D(n) - D(n-1) + 8ms**

How to get D_{pre} from EVG



- To get D_{pre} information from EVG, we realized it by transmitting via data buffer at shot#n-2 timing.
- When EVR received D_{pre}, it sets this value board register.
- In this specification, resolution(jitter) of 12 ms charging time reached at 30 ps. This value has almost no effect on beam jitter originated from kicker timing.

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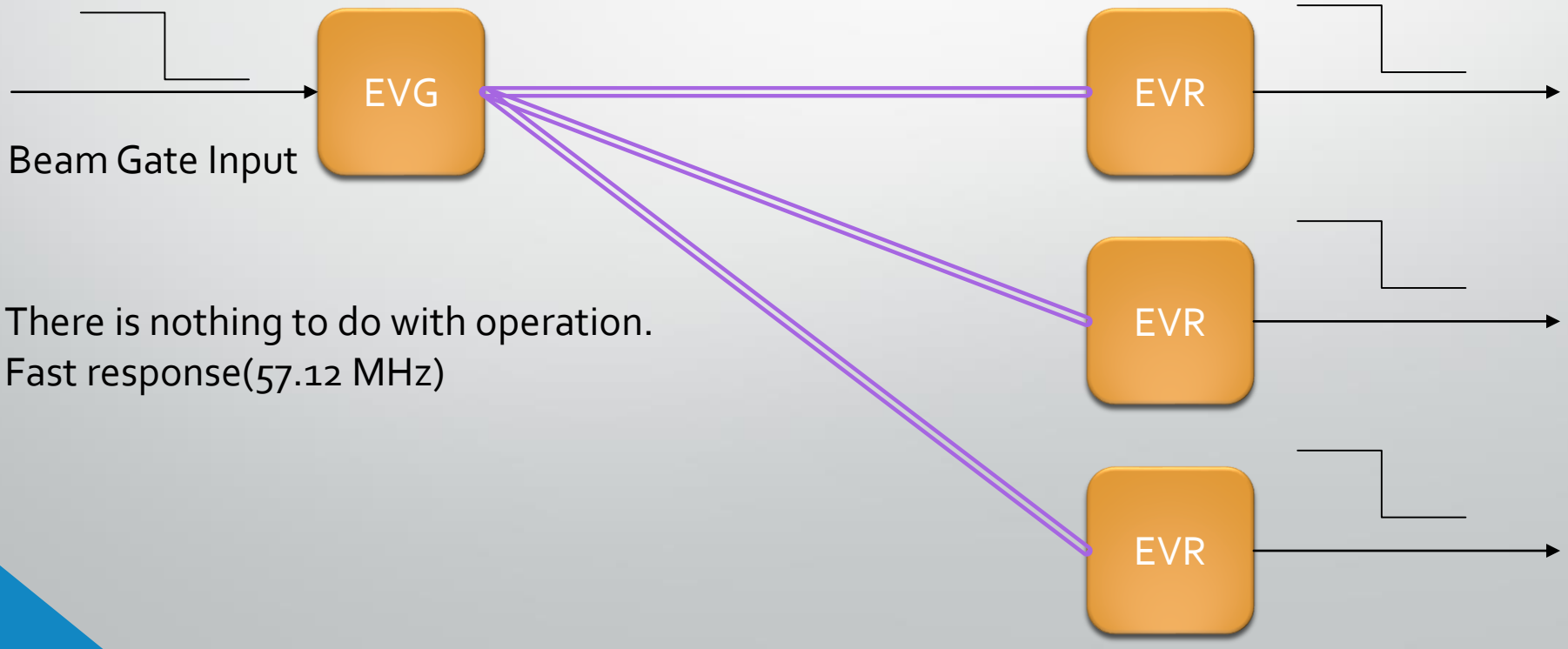
Beam Gate via Distributed Bus

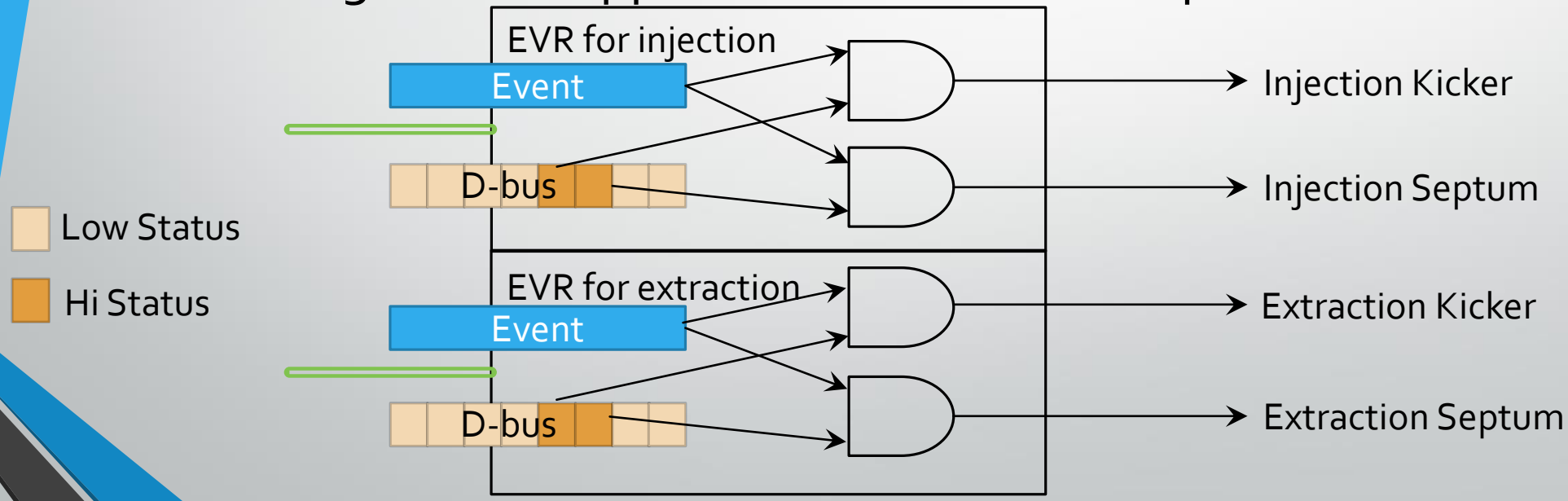
- We have developed beam gate transmitted by using 8-bit of distributed bus(D-bus).
- 8 kinds of logic level is available to transfer to EVR



- There is nothing to do with operation.
- Fast response(57.12 MHz)

Establishment of Injection/extraction control with D-bus beam gate

- We made it possible to control each injection/extraction kicker and septum by making AND logic D-bus beam gate and the Event in IOC.
- This Logic is also applied Gun and Kicker/Septum of LER and HER.



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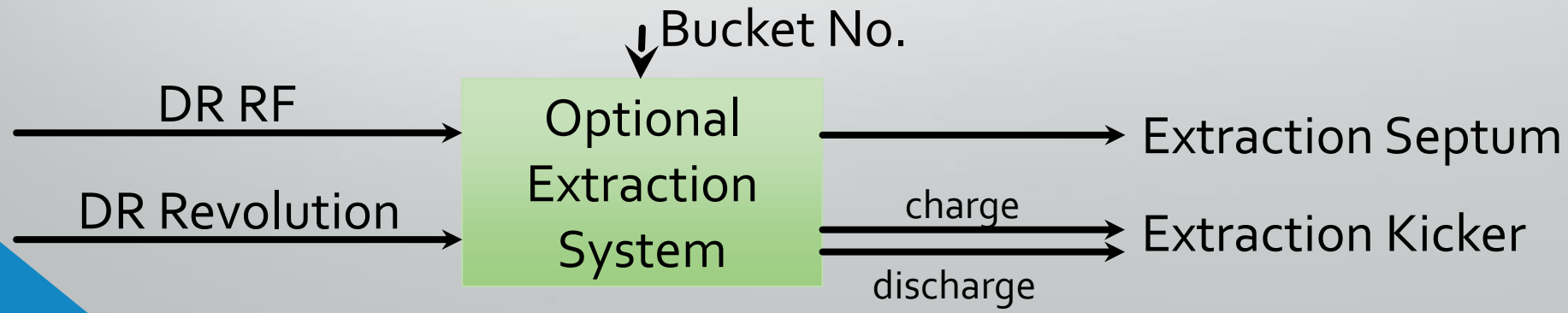
Optional Extraction System

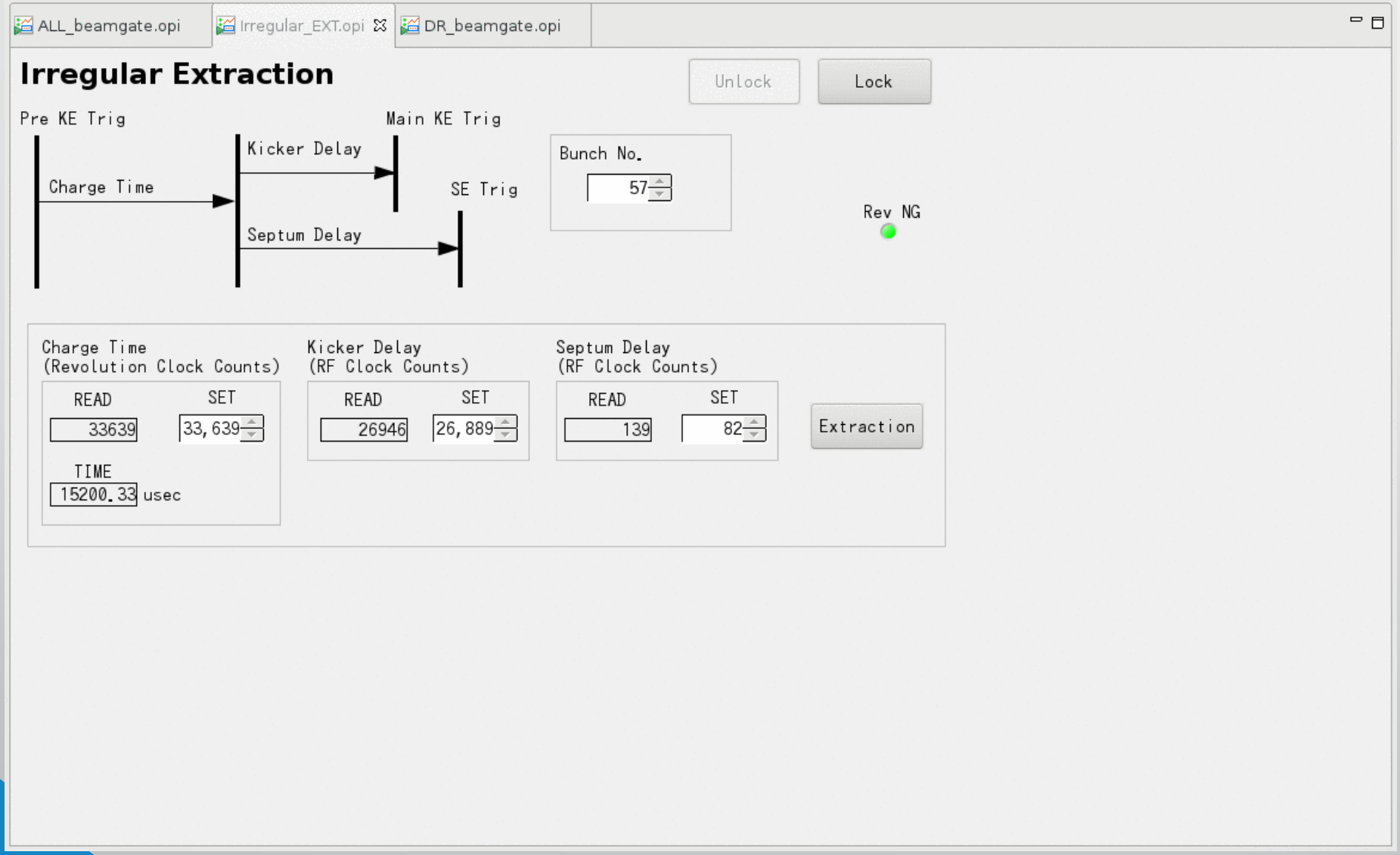
- We need to consider various situation to operate beam handling.

Among them …

- It is necessary to generate extraction trigger in the case of …
  - Extraction after changing DR RF for dispersion measurement
  - Extraction when LER abort
- In this case, Event Timing system cannot calculate reasonable extraction timing.
- For this purpose, Optional Extraction System has been developed.

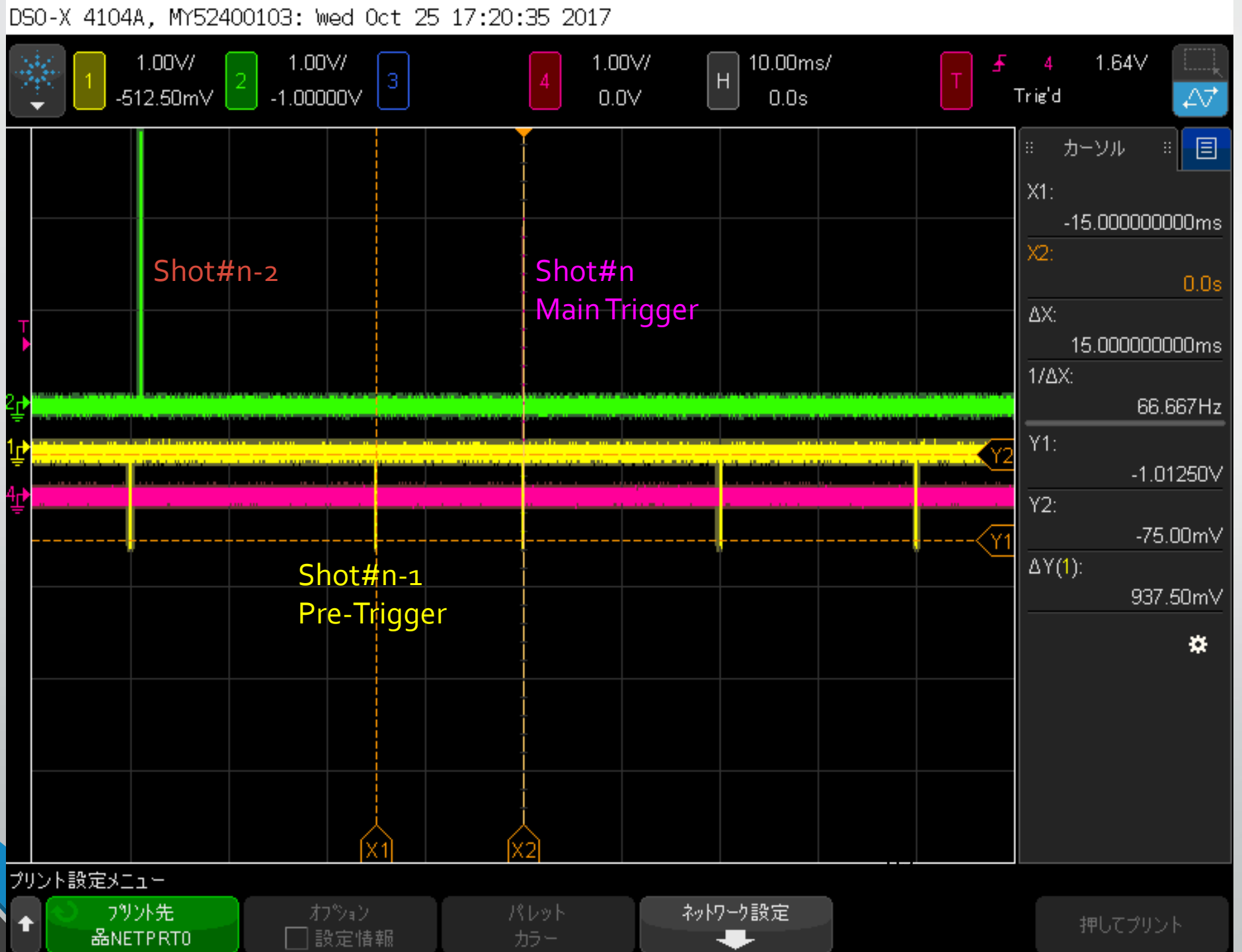


Optional Extraction System

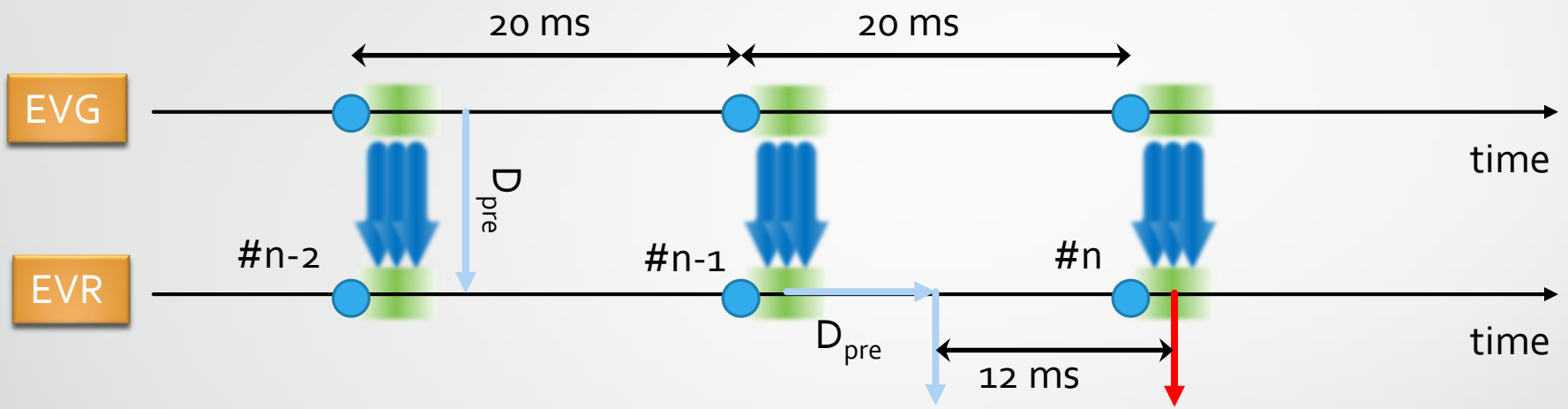


Summary and future

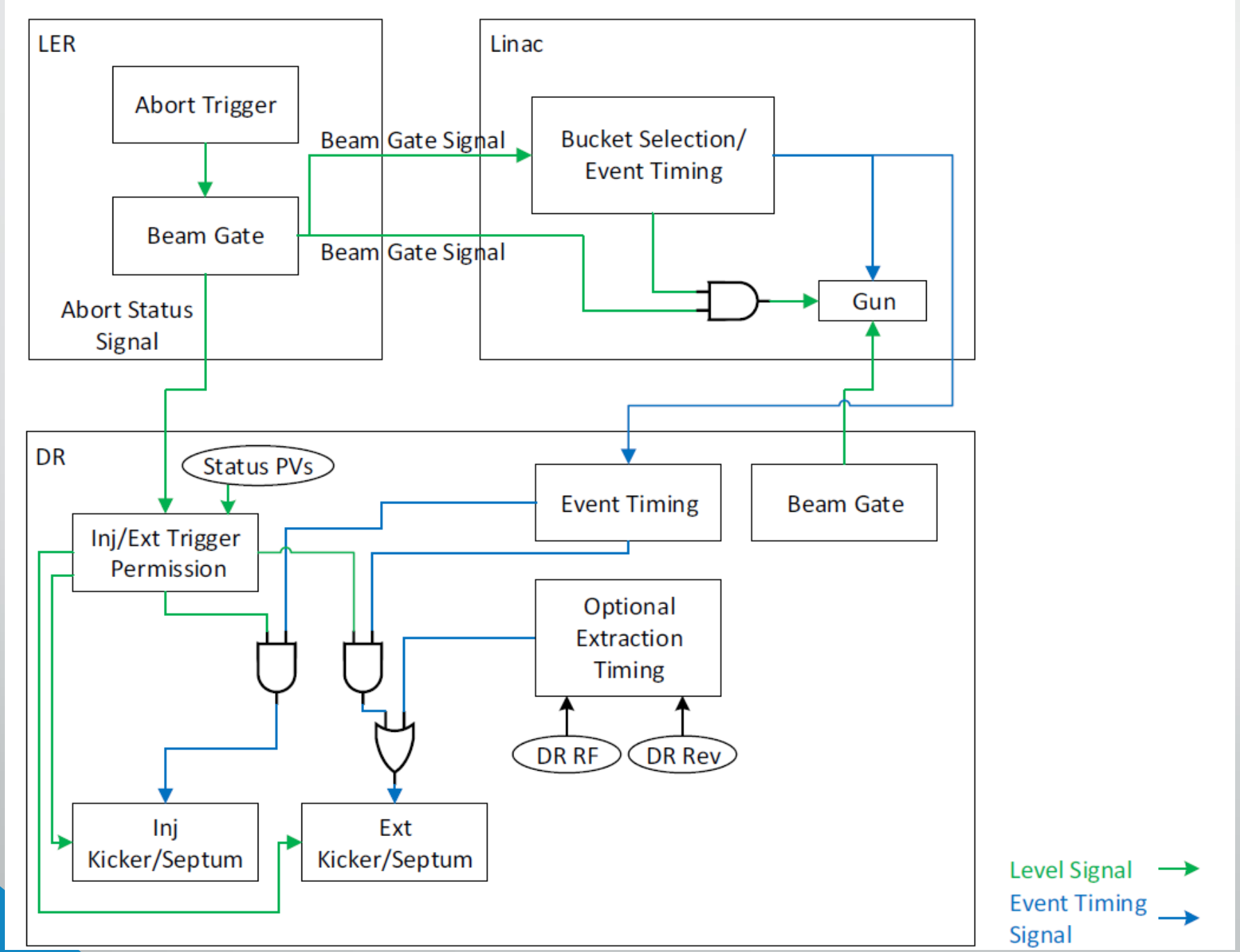
- DR sub-timing station was developed.
  - Event is received 2-EVRs and send to devices
  - Pre-Trigger generation with fixed time duration for Kicker magnets was succeeded by calculating at EVG and sending to EVR via data buffer.
- Optional Extraction system was developed.
- Beam Gate transmission via Distributed bus was succeeded
  - Injection and extraction control was well established.
- During only DR operation, this system has not hang up yet!


DSO-X 4104A, MY52400103: Wed Oct 25 17:20:35 2017
1.00V/
-512.50mV
1.00V/
-1.00000V
1.00V/
0.0V
10.00ms/
0.0s
Trig'd
1.64V
カーソル
X1:
-15.000000000ms
X2:
0.0s
ΔX:
15.000000000ms
1/ΔX:
66.667Hz
Y1:
-1.01250V
Y2:
-75.00mV
ΔY(1):
937.50mV
Shot#n-2
Shot#n
Main Trigger
Shot#n-1
Pre-Trigger
X1
X2
Y1
Y2
プリント設定メニュー
プリント先
NETPRT0
オプション
設定情報
パレット
カラー
ネットワーク設定
押してプリント

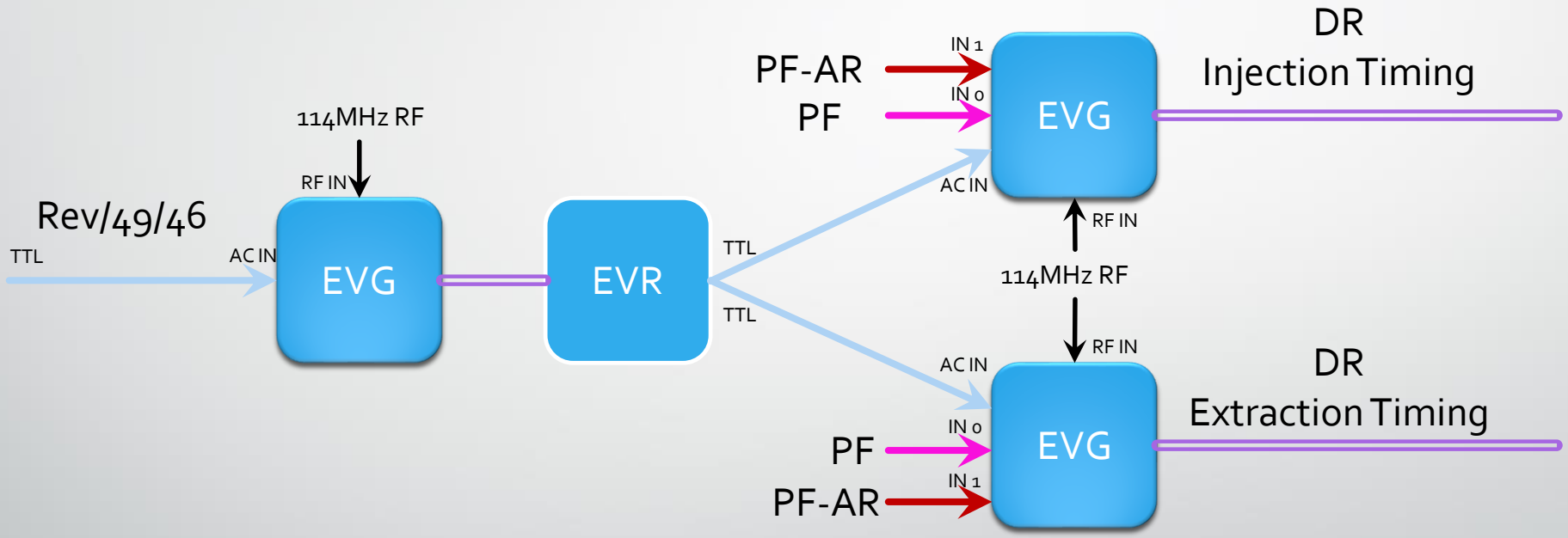
How to get D_{pre} from EVG to EVR



- Event code transmits every 20ms, and includes bucket selection delay within 2ms.
- Trigger timing to charge Kicker magnet has to send 12 ms before discharge timing.
- If discharge timing generates at shot #n, charge timing(pre-trigger) has to generate at shot #n-1
- To satisfy this situation,

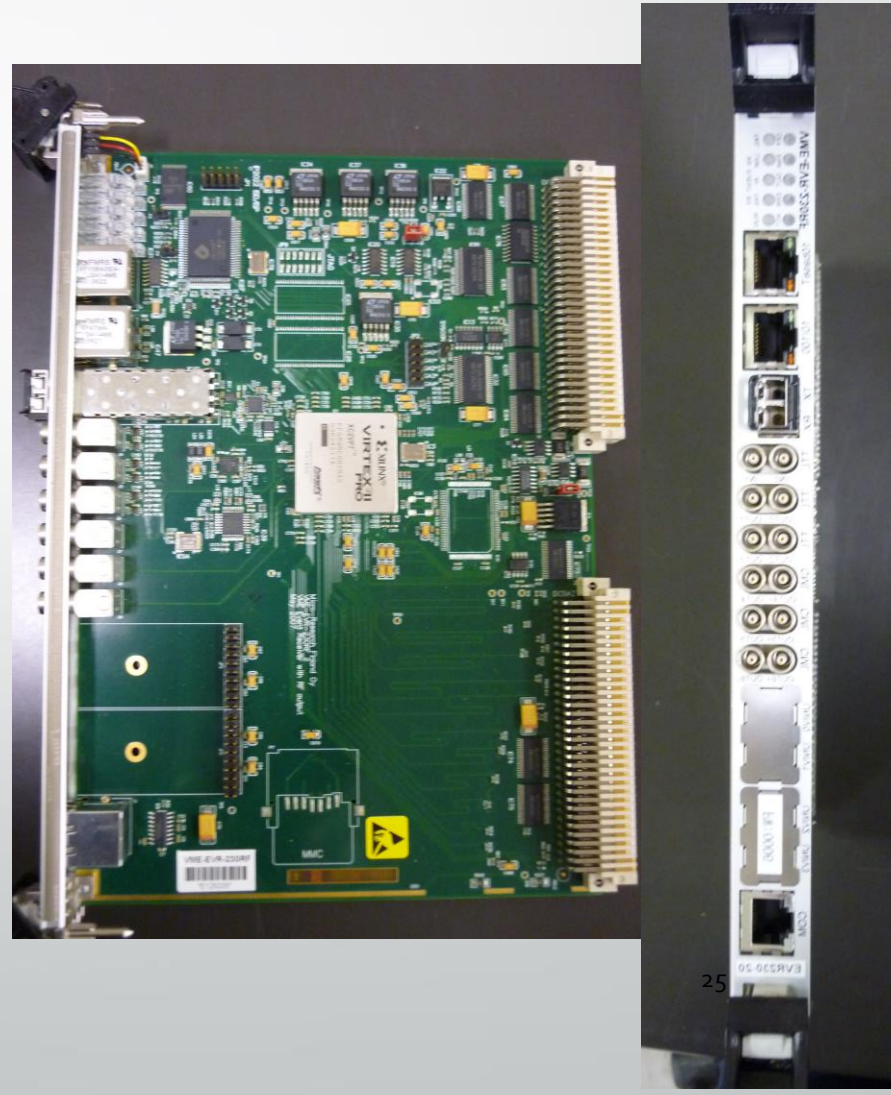

LER
Abort Trigger
Beam Gate
Abort Status Signal
Beam Gate Signal
Beam Gate Signal
Linac
Bucket Selection/ Event Timing
Gun
DR
Status PVs
Inj/Ext Trigger Permission
Event Timing
Beam Gate
Optional Extraction Timing
DR RF
DR Rev
Inj Kicker/Septum
Ext Kicker/Septum
Level Signal
Event Timing Signal

Master Event Timing system

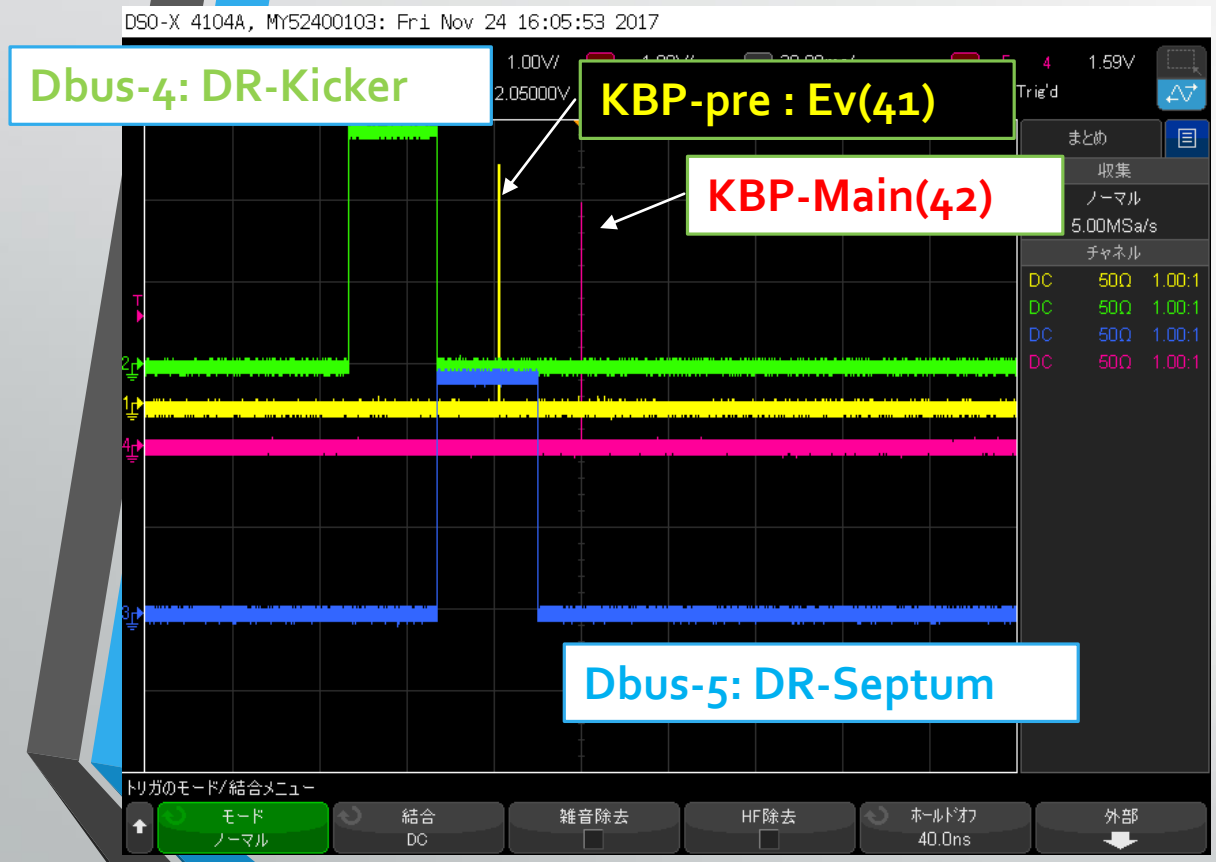


Specification of the VME-EVR-230RF

- FPGA:Vertex Ⅱ pro(XC2VP7)
- Bit rate 1.0 to 2.5 Gbps, event clock rate 50 MHz to 125 MHz
- Four programmable front panel TTL outputs
- Two front panel TTL inputs
- Three differential CML pattern outputs capable of RF recovery
- Two universal I/O slots
- Rear I/O
- Jitter typically < **15** ps rms for TTL outputs, < **5** ps rms for CML outputs



Beam Gate


DSO-X 4104A, MY52400103: Fri Nov 24 16:05:53 2017
Dbus-4: DR-Kicker
KBP-pre : Ev(41)
KBP-Main(42)
Dbus-5: DR-Septum
1.00V/
2.05000V
1.59V
Trig'd
まとめ
収集
ノーマル
5.00MSa/s
チャネル
DC 50Ω 1.00:1
DC 50Ω 1.00:1
DC 50Ω 1.00:1
DC 50Ω 1.00:1
トリガのモード/結合メニュー
モード
ノーマル
結合
DC
雑音除去
HF除去
ホールドオフ
40.0ns
外部